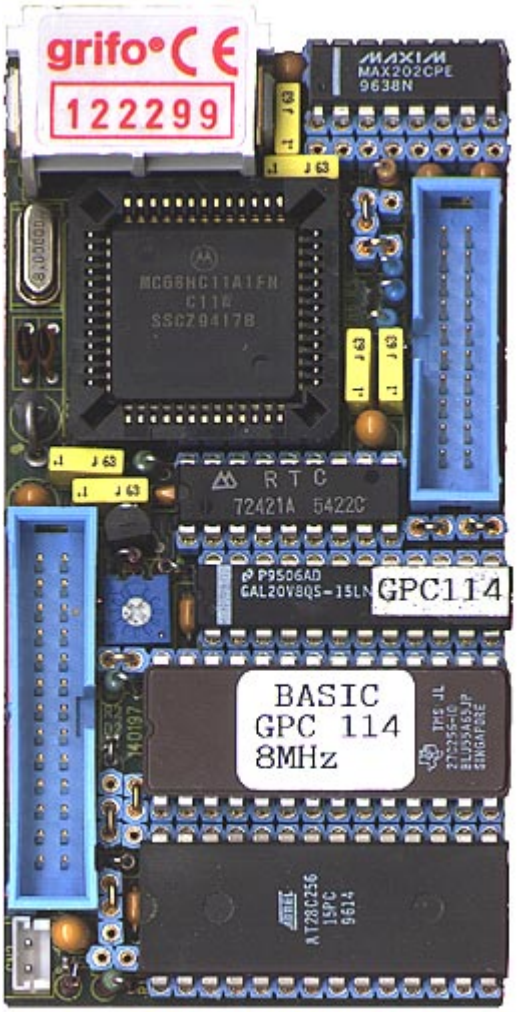
GPC® 114

General Purpose Controller 68 HC 11

MANUALE TECNICO



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GPC® 114 Edizione 3.20 *Rel. 9 Febbraio 1999*

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General Purpose Controller 68 HC 11

MANUALE TECNICO

Modulo Intelligente della serie **Abaco® BLOCK**, nel formato 100x50; contenitore, opzionale, per guide ad Ω tipo **DIN 46277-1** e **DIN 46277-2**; **CPU 68HC11A1**, con quarzo da **8 MHz**; indirizzamento massimo 64KBytes 32K RAM e zoccoli per 32K EPROM, 32K EEPROM, RAM o EPROM; circuiteria di **Back-Up** per **32K RAM**, tramite batteria al **LITIO** a bordo ed esterna; sofisticata circuiteria per la riconfigurazione del mappaggio delle risorse gestibile tramite due semplici jumpers; **E²** interna alla CPU da 512 Bytes; Orologio **RTC 71421A** con Batteria al **LITIO**, in grado di generare **INT**; 8 linee di **A/D** Converter da **8 Bits**, 12 µs, +2,5V di fondo scala; 10 linee TTL di I/O, settabili da software; 3 Timer-Input-Capture da 16 bits; 5 Timer Compare Output Register da 16 bits; 1 8 bit Pulse Accumulator Circuit; **Watch-Dog** settabile da software; Linea seriale in **RS232** oppure in RS422 o RS485; 1 Enhanced NRZ Serial Communication Interface (SCI); connettore di espansione per **Abaco® I/O BUS** da 26 vie; connettore standard di **I/O** da 20 vie; possibilità di funzionamento in **Wait-Mode, Stop-Mode**; unica tensione di alimentazione da 5 Vdc, 88 mA; protezione della logica di bordo dai transienti tramite **TransZorb™**; vasta disponibilità di software di sviluppo quali **Monitor, Debugger, Assembler, GET 11 e BASIC Interpretato, FORTH, Compilatore C, HTC-11, Kernel, Control PASCAL**, ecc.

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IMPORTANTE

Tutte le informazioni contenute in questo manuale sono state accuratamente verificate, ciononostante **grifo**® non si assume nessuna responsabilità per danni diretti o indiretti a cose e/o persone derivanti da errori tecnici ed omissioni o dall'uso del presente manuale, del software o dell' hardware ad esso associato.
grifo® altresi si riserva il diritto di modificare il contenuto e la veste di questo manuale senza alcun preavviso, con l' intento di offrire un prodotto sempre migliore, senza che questo rappresenti un obbligo per **grifo**®.
Per le informazioni specifiche sui componenti montati sulla scheda, l'utente deve fare riferimento ai Data Book delle case costruttrici o delle seconde sorgenti.

LEGENDA SIMBOLI

Nel presente manuale possono comparire i seguenti simboli:

Attenzione: Pericolo generico

Attenzione: Pericolo di alta tensione

Marchi Registrati

INDICE GENERALE

INDICE DELLE FIGURE

INTRODUZIONE

L'uso di questi dispositivi è rivolto - IN VIA ESCLUSIVA - a personale specializzato.

Scopo di questo manuale è la trasmissione delle informazioni necessarie all'uso competente e sicuro dei prodotti. Esse sono il frutto di un'elaborazione continua e sistematica di dati e prove tecniche registrate e validate dal Costruttore, in attuazione alle procedure interne di sicurezza e qualità dell'informazione.

I dati di seguito riportati sono destinati - IN VIA ESCLUSIVA - ad un utenza specializzata, in grado di interagire con i prodotti in condizioni di sicurezza per le persone, per la macchina e per l'ambiente, interpretando un'elementare diagnostica dei guasti e delle condizioni di funzionamento anomale e compiendo semplici operazioni di verifica funzionale, nel pieno rispetto delle norme di sicurezza e salute vigenti.

Le informazioni riguardanti installazione, montaggio, smontaggio, manutenzione, aggiustaggio, riparazione ed installazione di eventuali accessori, dispositivi ed attrezzature, sono destinate - e quindi eseguibili - sempre ed in via esclusiva da personale specializzato avvertito ed istruito, o direttamente dall'ASSISTENZA TECNICA AUTORIZZATA, nel pieno rispetto delle raccomandazioni trasmesse dal costruttore e delle norme di sicurezza e salute vigenti.

I dispositivi non possono essere utilizzati all'aperto. Si deve sempre provvedere ad inserire i moduli all'interno di un contenitore a norme di sicurezza che rispetti le vigenti normative. La protezione di questo contenitore non si deve limitare ai soli agenti atmosferici, bensì anche a quelli meccanici, elettrici, magnetici, ecc.

Per un corretto rapporto coi prodotti, è necessario garantire leggibilità e conservazione del manuale, anche per futuri riferimenti. In caso di deterioramento o più semplicemente per ragioni di approfondimento tecnico ed operativo, consultare direttamente l'Assistenza Tecnica autorizzata.

Al fine di non incontrare problemi nell'uso di tali dispositivi, è conveniente che l'utente - PRIMA DI COMINCIARE AD OPERARE - legga con attenzione tutte le informazioni contenute in questo manuale. In una seconda fase, per rintracciare più facilmente le informazioni necessarie, si può fare riferimento all'indice generale e all'indice analitico, posti rispettivamente all'inizio ed alla fine del manuale.

VERSIONE SCHEDA

Il presente manuale è riferito alla scheda **GPC® 114** versione **100997** e sucessive. La validità delle informazioni riportate è quindi subordinata al numero di versione della scheda in uso e l'utente deve quindi sempre verificare la giusta coriispondenza tra le due indicazioni. Sulla scheda il numero di versione è riportato in più punti sia a livello di serigrafia che di stampato (ad esempio vicino al resistore R2 ed al diodo D2 nel lato componenti).

CARATTERISTICHE GENERALI

La scheda **GPC® 114** è un potente modulo di controllo, della fascia **Low-Cost** con consumi estremamente ridotti, in grado di funzionare autonomamente e/o come periferica intelligente e/o remotata in una più vasta rete di telecontrollo e/o di acquisizione. Fa parte della **Serie 4** di CPU, nel formato **BLOCK**, con ingombro di soli 100x50 mm.
La **GPC® 114** può essere fornita di un supporto in plastica provvisto degli attacchi per le guide ad **Omega** tipo **DIN 46277-1** e **DIN 46277-2**. In questo modo non è necessario l'uso di un **Rack**, ma la scheda può essere montata, in modo più economico, direttamente nel quadro elettrico. Viste le ridotte dimensioni della scheda **GPC® 114**, questa può essere montata nella stessa guida in plastica che contiene le periferiche di I/O, come ad esempio la **ZBR 84** , formando in questo modo un unico elemento **BLOCK**. Un'altra tipica applicazione della scheda **GPC® 114**, è quella di essere adoperata come un modulo di CPU da montare in **Piggy-Back** sulle schede periferiche realizzate direttamente dall'utente.
Sono disponibili diversi Tools di sviluppo software che consentono di poter usare la scheda come sistema di sviluppo di se stessa, sia in Assembler che con linguaggi evoluti. Una particolare menzione và ai Tools di sviluppo quali i vari **Compilatori C**, il **FORTH**, vari **Real-Time** ed il comodo **BASIC 11**.
Il **BASIC 11**, oltre alla nota facilità di Debugger, consente di programmare direttamente a bordo scheda una **EEPROM** con il programma utente.
La **GPC® 114** è dotata di una serie di connettori normalizzati, standard **Abaco®**, che le consentono di utilizzare immediatamente la numerosa serie di moduli **BLOCK** di I/O oppure le permettono il collegamento, in modo molto semplice ed economico, delle interfacce da campo costruite direttamente dall'utente o da terze parti.
Per una rapida prototipizzazione si può ricorrere alle ottime schede **SPA 03** ed **SPA 04** su cui è possibile montare, anche in **Piggy-Back**, la **GPC® 114**. La presenza del connettore **Abaco® I/O BUS** consente inoltre di poter pilotare direttamente le schede di I/O tipo **ZBR 84**, **ZBR 168**, **ZBR 246**, **ZBR 324**, **ZBT 84**, **ZBT 168**, **ZBT 246**, **ZBT 324**, e tramite **ABB 03**, **ABB 05**, ecc. è possibile gestire tutte le numerose schede periferiche disponibili sul **BUS Abaco®**.

- Modulo Intelligente della serie **Abaco® BLOCK**, nel formato 100x50
- Contenitore, opzionale, per guide ad Ω tipo **DIN 46277-1** e **DIN 46277-2**
- **CPU 68HC11A1**, con quarzo da **8 MHz**
- Indirizzamento massimo 64KBytes
- 32K RAM e zoccoli per 32K EPROM, 32K EEPROM, RAM o EPROM
- Circuiteria di **Back-Up** per **32K RAM**, tramite batteria al **LITIO** a bordo ed esterna
- Sofisticata circuiteria per la riconfigurazione del mappaggio delle risorse gestibile tramite due semplici jumpers
- **E²** interna alla CPU da 512 Bytes
- Orologio **RTC 71421A** con Batteria al **LITIO**, in grado di generare **INT**
- 8 linee di **A/D** Converter da **8 Bits**, 12 µs, +2,49V o 5,00V di fondo scala
- 10 linee TTL di I/O, settabili da software; jumper per RUN/DEBUG Mode
- 3 Timer-Input-Capture da 16 bits; 5 Timer Compare Output Register da 16 bits
- 1 8 bit Pulse Accumulator Circuit
- **Watch-Dog** settabile da software
- Linea seriale in **RS232** oppure in RS422 o RS485
- 1 Enhanced NRZ Serial Communication Interface (SCI)
- Connettore di espansione per **Abaco® I/O BUS** da 26 vie
- Connettore standard di **I/O** da 20 vie
- Possibilità di funzionamento in **Wait-Mode, Stop-Mode**
- Unica tensione di alimentazione da 5 Vdc, 88 mA
- Protezione della logica di bordo dai transienti tramite **TransZorb™**
- Vasta disponibilità di software di sviluppo quali **Monitor, Debugger, Assembler, GET 11 e BASIC Interpretato, FORTH, Compilatore C, HTC-11, Kernel, Control PASCAL**, ecc.

PROCESSORE DI BORDO

La scheda **GPC® 114** e' predisposta per accettare il processore MC68HC11A1 prodotto dalla MOTOROLA, il quale ha le seguenti caratteristiche di massima:

- no ROM, no EPROM
- processore ad 8 bit
- 512 bytes di EEPROM
- 256 bytes di RAM interna
- 16 linee di I/O digitale
- 8 linee di A/D converter ad 8 bit
- 1 linea per la comunicazione seriale
- 1 timer counter a 16 bit
- 1 Watch Dog gestibile via software
- Software Buffalo interno, settare JS5 chiuso e JS20 aperto

Per maggiori informazioni a riguardo di questo componente si faccia riferimento all'apposita documentazione della casa costruttrice.

DISPOSITIVI DI CLOCK

Sulla **GPC® 114** il segnale di clock è generato da un quarzo presente sulla scheda, che fornisce una frequenza di 8 MHZ. Tale frequenza, opportunamente divisa, genera la frequenza di clock della CPU da 2 MHz, quindi tutte le eventuali tempistiche devono essere calcolate a partire da questi valori.

COMUNICAZIONE SERIALE

La comunicazione seriale è completamente settabile via software per quanto riguarda sia il protocollo, sia la velocita' di comunicazione, che puo' raggiungere un massimo di 125 KBaud. La comunicazione con il mondo esterno avviene in Full Duplex, utilizzando il protocollo di comunicazione RS 232 o RS 422-485; la scelta del protocollo elettrico viene effettuata configurando alcuni jumpers.

ALIMENTAZIONE

L' unica tensione di alimentazione necessaria è di **+5 Vdc che deve essere fornita tramite i pin 25 (GND) e 26 (+5Vdc) di CN1**. Sulla scheda sono state adottate tutte le scelte circuitali e componentistiche che tendono a ridurre i consumi, compresa la possibilità di far lavorare alcuni microcontrollori in power down ed idle mode ed a ridurre la sensibilità ai disturbi. Si ricorda inoltre che è presente una circuiteria di protezione tramite **TransZorb™** per evitare danni dovuti a tensioni non corrette.

LOGICA DI CONTROLLO

Il mappaggio di tutti i registri delle periferiche presenti sulla scheda e dei dispositivi di memoria, è affidata ad un'opportuna logica di controllo che si occupa di allocare tali dispositivi nello spazio d'indirizzamento della CPU, tutto questo avviene settando opportunamente jumpers.
Per maggiori informazioni fare riferimento al paragrafo "MAPPAGGIO DELL'I/O".

DISPOSITIVI DI MEMORIA

E' possibile dotare la scheda di un massimo di 64K bytes di memoria variamente suddivisi con un massimo di 32K EPROM, 32K RAM, 32K RAM/EEPROM/EPROM. La scelta della configurazione delle memorie presenti sulla scheda può avvenire in relazione all'applicazione da risolvere e quindi in relazione alle esigenze dell'utente. Da questo punto di vista si ricorda che la scheda viene normalmente fornita con i 32K RAM sldati di lavoro e che tutte le rimanenti memorie devono essere quindi opportunamente specificate in fase di ordine della scheda, vedi figura 14.
Tramite la circuiteria di back up presente a bordo scheda c'è inoltre la possibilità di tamponare fino ad un massimo di 32K RAM aggiungendo quindi la possibilità di mantenere i dati anche in assenza di alimentazione. Questa caratteristica fornisce alla scheda la possibilità di ricordare in ogni condizione, una serie di parametri come ad esempio la configurazione o lo stato del sistema. La circuiteria di back up è basata su una batteria al Litio presente a bordo scheda e da una batteria esterna collegabile tramite un apposito connettore. Qualora la quantità di RAM tamponata risulti insufficiente (ad esempio per sistemi di data loghin) si possono sempre utilizzare i moduli di RAM tamponata e/o di EEPROM.
Il mappaggio delle risorse di memoria avviene tramite una opportuna circuiteria di bordo, che provvede ad allocare i dispositivi all'interno dello spazio d'indirizzamento del microprocessore; tale logica di controllo provvede a gestire in modo completamente automatico diversi tipi di mappaggi che si adattano ai diversi pacchetti software disponibili per la **GPC® 114**.
Per maggiori informazioni fare riferimento al capitolo DESCRIZIONE HARDWARE" e DESCRIZIONE SOFTWARE DELLE PERIFERICHE DI BORDO". Per una descrizione più approfondita sui dispositivi di memoria, sugli zoccoli da utilizzare e sullo strippaggio della scheda, fare riferimento al paragrafo "SELEZIONE MEMORIE".

ABACO® I/O BUS

Una delle caratteristiche di fondamentale importanza della **GPC® 114** è quella di disporre del cosiddetto **ABACO® I/O BUS**: ovvero un connettore normalizzato **ABACO®** con cui è possibile collegare la scheda ad una serie di moduli esterni intelligenti e non. Tra questi si trovano moduli per acquisizione di segnali analogici (A/D come **ABC 04** o **ABB 08**), per la generazione di segnali analogici (D/A), per gestione di linee di I/O logico, per counter, ecc. e ne possono essere realizzati anche su specifiche richieste dell'utente. Utilizzando mother board come l'**ABB 03** o l'**ABB 05** è inoltre possibile gestire tutte le schede periferiche in formato europa con interfaccia per BUS **ABACO®**. Tale caratteristica rende la scheda espandibile con un'ottimo rapporto prezzo/prestazioni e quindi adatta a risolvere molti dei problemi dell'automazione industriale.

CONTATTO DI RESET

Sulla **GPC® 114** è presente un contatto di reset (P1) che ha la funzione di resettare e quindi far ripartire la scheda da una condizione di azzeramento generale. La funzione principale di questo contatto è quella di uscire da condizioni di loop infinito, soprattutto durante la fase di debug o di garantire uno stato certo di partenza. Per una facile individuazione di tale contatto di reset a bordo scheda, si faccia riferimento alla figura 14.

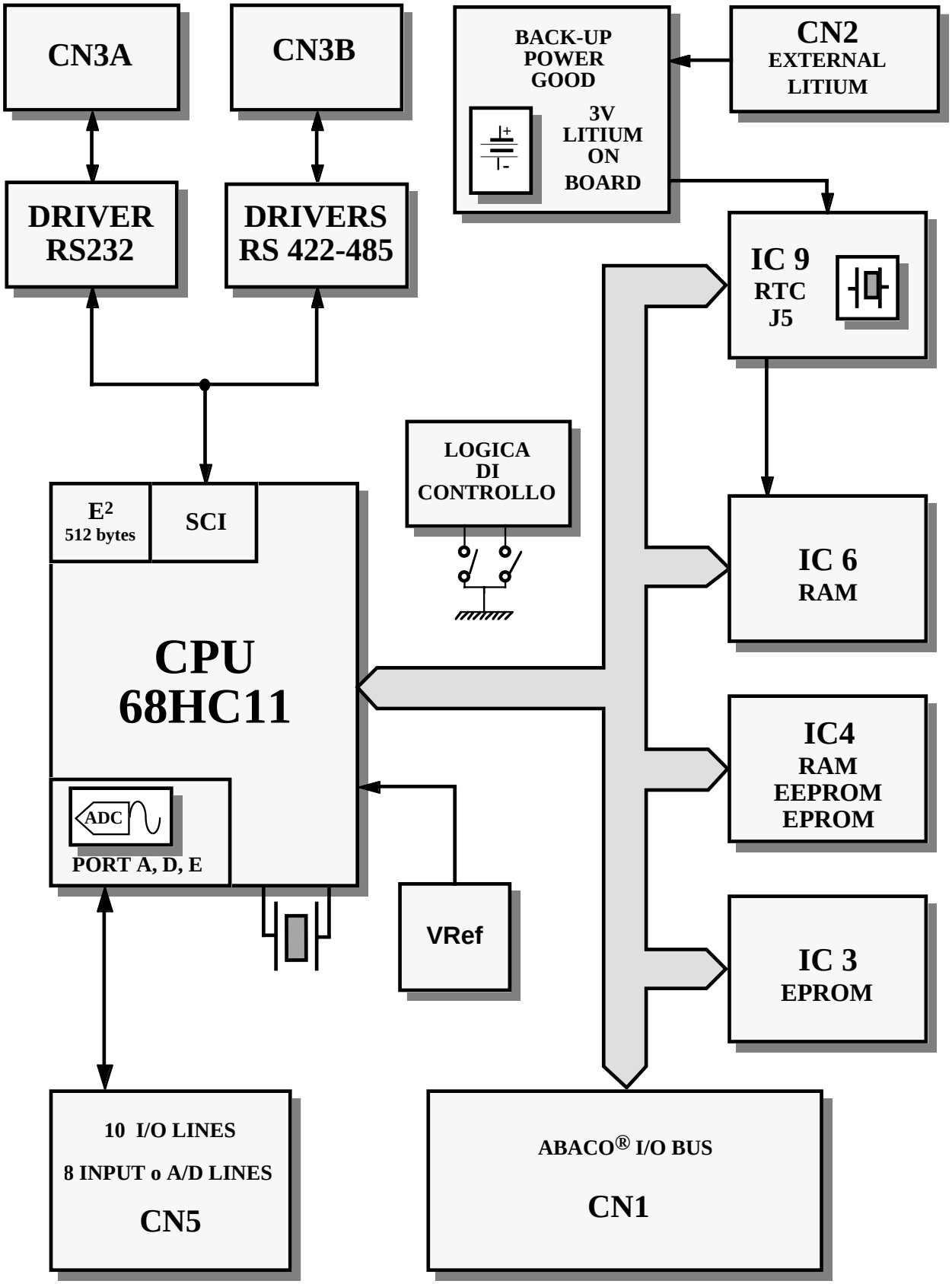


FIGURA 1: SCHEMA A BLOCCHI

DISPOSITIVI PERIFERICI DI BORDO

La scheda **GPC® 114**, nata per risolvere molteplici problemi di controllo e comando di automatismi, è dotata di alcuni componenti periferici che si occupano dell'interfacciamento con il mondo esterno. In particolare:

- **SCI**: periferica interna alla CPU in grado di gestire una linea per la comunicazione seriale. Il dispositivo può essere utilizzato per la comunicazione con tutti i sistemi provvisti di una linea seriale bufferata in RS 232 o RS 422-485. Dal punto di vista software è infatti definibile la velocità di comunicazione, la lunghezza della parola, il numero di stop bit, la parità e lo stato dei segnali di handshake hardware. Il tutto avviene tramite una semplice programmazione di registri interni alla CPU dove però il baud rate è in funzione del quarzo che si stà utilizzando.

-**A/D converter**: periferica interna alla CPU in grado di acquisire 8 canali con una risoluzione massima di 8 bits. Dal punto di vista software è possibili definire quali canali attivare, dare lo start o lo stop all' acquisizione ecc. Al fine di semplificare la gestione dello stesso A/D alcuni pacchetti software forniscono delle procedure di utility che gestiscono la sezione in tutte le sue parti. I segnali analogici collegabili sono segnali in tensione variabili nel range 0÷2,490V.

-**COP**: periferica interna alla CPU che permette il reset della medesima ad intervalli di tempi prefissati se non viene effettuato un retrigger, in pratica è un vero e proprio watchdog. Dal punto di vista software è definibile il tempo di intervento e l' abilitazione.

- **Real Time Clock 72421**: permette di prelevare l'orario (ore, minuti, secondi) ed il calendario (girno, mese, anno, giorno della settimana).

- **EEPROM**: periferica interna alla CPU è molto utile in caso si debbano mantenere delle informazioni anche in assenza di alimentazione, senza ricorrere al back up della RAM, con una sicurezza estrema sulla validità dei dati. Tale modulo hae un size di 512 bytes.

Per ulteriori informazioni a riguardo dei dispositivi periferici descritti, si faccia riferimento alla documentazione tecnica della casa costruttrice.

INTERFACCIA DI I/O

Tramite CN5 (connettore standard di **I/O**) si può collegare la **GPC® 114** ai numerosi moduli del carteggio **grifo®** che riportano lo stesso pin out. Di particolare interesse è la possibilità di collegare direttamente una serie di moduli come la **XBY R4**, **OBI 01**, **OBI P8**, ecc. con cui risolvere tutti i problemi di interfacciamento con il campo. Questi moduli sono già dotati delle risorse necessarie per gestire ingressi optoisolati ed uscite a relè o transistor .
Dal punto di vista dell'installazione, queste interfaccie richiedono un solo flat a 20 vie con cui è possibile portare anche le alimentazioni, mentre dal punto di vista software la gestione è altrettanto semplice ed immediata, infatti i pacchetti software disponibili per la **GPC® 114** sono provvisti di tutte le procedure necessarie.

SPECIFICHE TECNICHE

CARATTERISTICHE GENERALI

Risorse di bordo	16 Input/Output programmabili TTL 1 Timer Counter a 16 bit 1 Linee bidirezionali RS 232 o 422-485 1 Watch Dog 8 Linee di A/D converter 1 Real Time Clock 1 Contatto locale di reset 1 Input utente leggibile da software (J5) 1 Connettore di espansione per Abaco® I/O BUS
Memoria indirizzabile	IC 3:EPROM da 32K x 8 IC 6:RAM da 32K x 8 saldata IC 4:RAM/EEPROM//EPROM da 8K x 8 a 32K x 8
CPU di bordo	Motorola Famiglia M6801 (68HC11A1)
Frequenza di clock	8 MHz
Risoluzione A/D	8 bits
Tempo conversione A/D	12 µs

CARATTERISTICHE FISICHE

Dimensioni	100 x 50 x 25 mm 110 x 60 x 60 mm	(senza contenitore) (con contenitore per guide DIN)
Peso	74 g. 134 g	(senza contenitore) (con contenitore per guide DIN)
Connettori	CN1: 26 vie scatolino verticale M CN2: 2 vie verticale M CN3A: PLUG a 6 vie CN3B: PLUG a 6 vie CN5: 20 vie scatolino verticale M	
Range di temperatura	da 0 a 50 gradi Centigradi	
Umidità relativa	20% fino a 90%	(senza condensa)
Tempo intervento watch dog	1049 msec 16,384 msec	(tempo lungo) (tempo corto)

CARATTERISTICHE ELETTRICHE

Tensione di alimentazione	+5 Vdc	
Corrente assorbita sui 5 Vdc	88 mA	
Batteria di bordo di back up:	3,0 Vdc; 180 mAh	
Batteria esterna di back up	3,6÷5 Vdc	
Corrente di back up	15µ A	
Ingressi analogici in tensione	0÷2,49 V; 0÷5,00 V	
Impedenza ingressi analogici	10 KΩ	
Rete terminazione RS 422-485:	Resistenza terminazione linea=	120 Ω
	Resistenza di pull up sul positivo=	3,3 KΩ
	Resistenza di pull down sul negativo=	3,3 KΩ

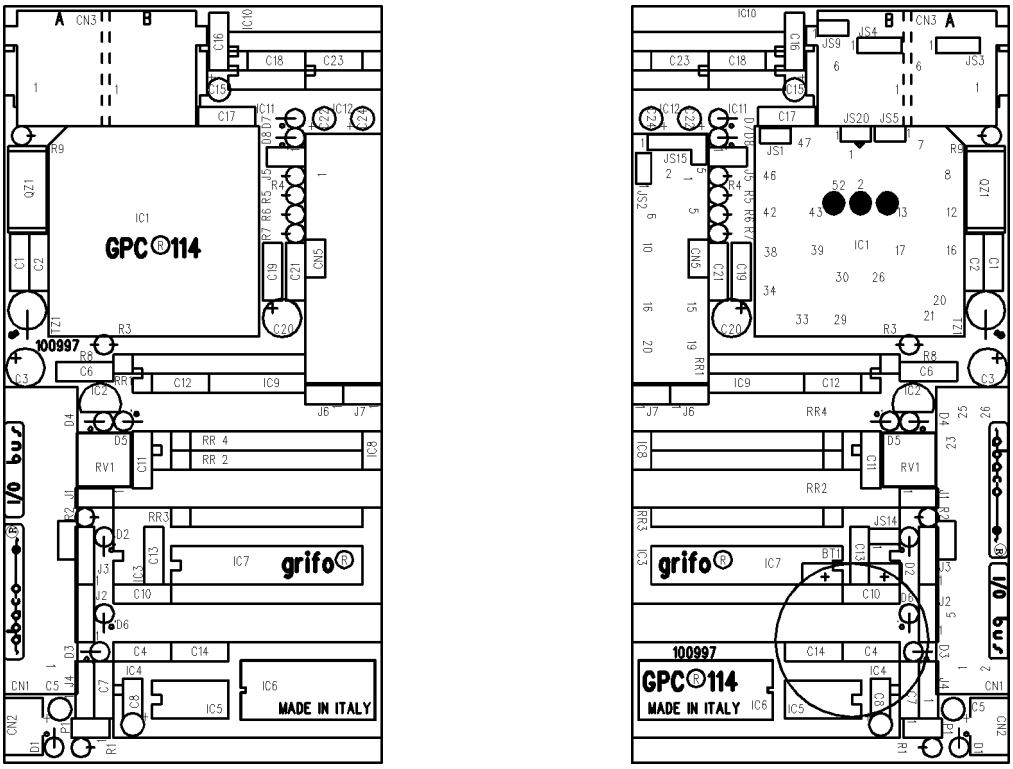


FIGURA 2: PIANTA COMPONENTI LATO COMPONENTI E LATO STAGNATURA

INSTALLAZIONE

In questo capitolo saranno illustrate tutte le operazioni da effettuare per il corretto utilizzo della scheda. A questo scopo viene riportata l'ubicazione e la funzione degli strips e dei connettori.

CONNESSIONI CON IL MONDO ESTERNO

Il modulo **GPC®114** è provvisto di 6 connettori con cui vengono effettuate tutte le connessioni con il campo e con le altre schede del sistema di controllo da realizzare. Di seguito viene riportato il loro pin-out ed il significato dei segnali collegati; per una facile individuazione di tali connettori, si faccia riferimento alla figura 14, mentre per ulteriori informazioni a riguardo del tipo di connessioni, fare riferimento alle figure successive che illustrano il tipo di collegamento effettuato a bordo scheda.

CN2 - CONNETTORE PER BATTERIA ESTERNA DI BACK UP

CN2 è un connettore a scatolino, verticale, maschio, con passo 2,54mm a 2 vie. Tramite CN2 deve essere collegata una batteria esterna che provvede a mantenere i dati della RAM di bordo (IC6), RTC (IC9) anche in assenza di tensione di alimentazione (per maggiori informazioni fare riferimento al paragrafo "BACK UP".

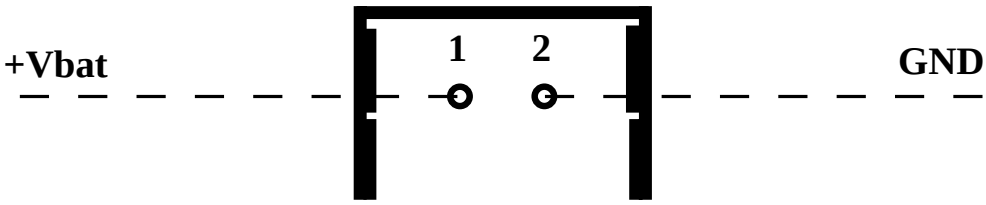


FIGURA 3: CN2 - CONNETTORE PER BATTERIA ESTERNA DI BACK UP

Legenda

+Vbat	=	I	-	Positivo della batteria esterna di back up
GND	=		-	Negativo della batteria esterna di back up

CN1 - CONNETTORE PER ABACO® I/O BUS (CONNETTORE DI ALIMENTAZIONE)

CN1 è un connettore a scatolino verticale con passo 2.54 mm a 26 piedini. Tramite CN1 si effettua la connessione tra la scheda e la serie di moduli esterni di espansione, da utilizzare per l'interfacciamento diretto con il campo. Tale collegamento è effettuato tramite l' **ABACO® I/O BUS** di cui questo connettore riporta tutti i segnali a livello TTL.

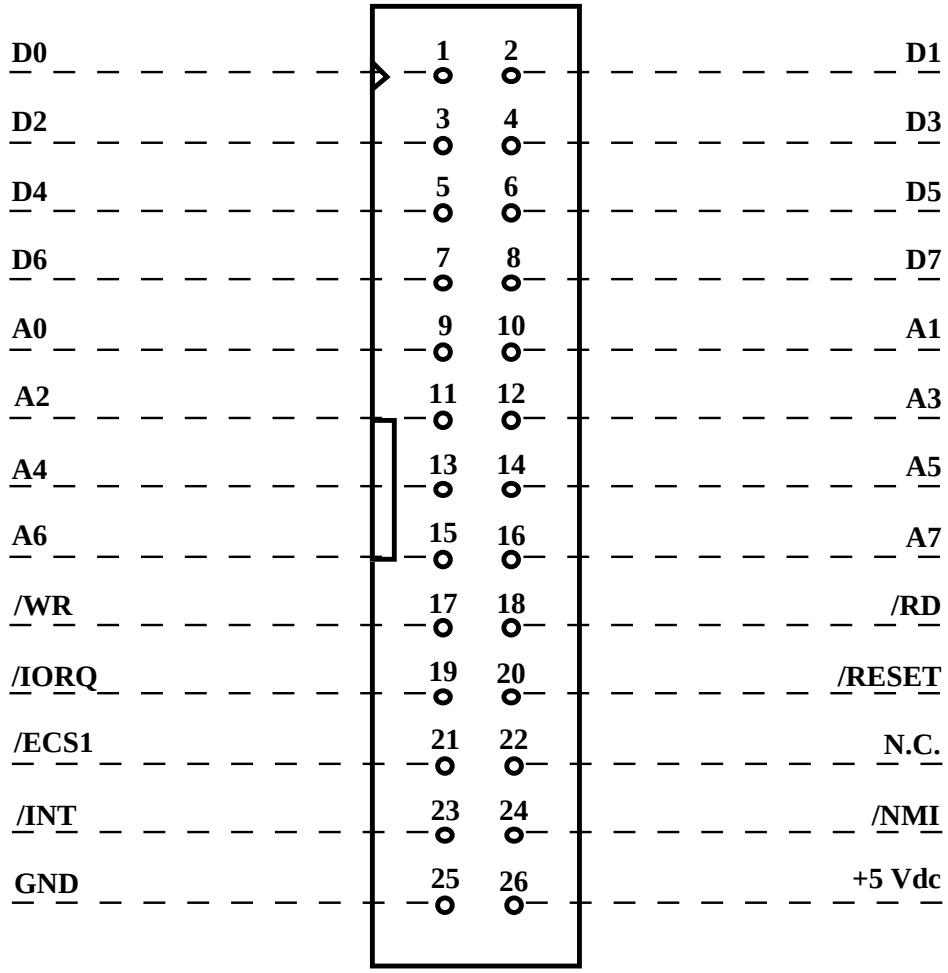


FIGURA 4: CN1 - CONNETTORE PER ABACO® I/O BUS

Legenda:

A0-A7	=	O	-	Address BUS: BUS degli indirizzi.
D0-D7	=	I/O	-	Data BUS: BUS dei dati.
/INT	=	I	-	Interrupt request: richiesta d'interrupt. Deve essere in open collector
/NMI	=	I	-	Non Mascable Interrupt: richiesta d'interrupt non mascherabile.
/IORQ	=	O	-	Input Output Request: richiesta operazione Input Output su I/O BUS.
/RD	=	O	-	Read cycle status: richiesta di lettura.
/WR	=	O	-	Write cycle status: richiesta di scrittura.
/RESET	=	O	-	Reset: azzeramento.
/ECS1	=	O	-	External Chip Select 1: abilitazione decodificata per 1 periferica esterna.
+5 Vdc	=	I/O	-	Linea di alimentazione a +5 Vdc.
GND	=		-	Linea di massa.
N.C.	=		-	Non Collegato.

CN5 - CONNETTORE PER I/O, A/D DELLA CPU.

CN5 è un connettore a scatolino verticale con passo 2.54 mm a 20 piedini. Tramite CN5 si effettua la connessione tra i port A , D e E della CPU, con l'ambiente esterno. Inoltre sono presenti 8 linee di INPUT per la sezione di A/D della CPU nel port E. Da ricordare che il port E della CPU ha una doppia funzione ossia le 8 linee possono essere ingressi digitali o ingressi per l' A/D converter.

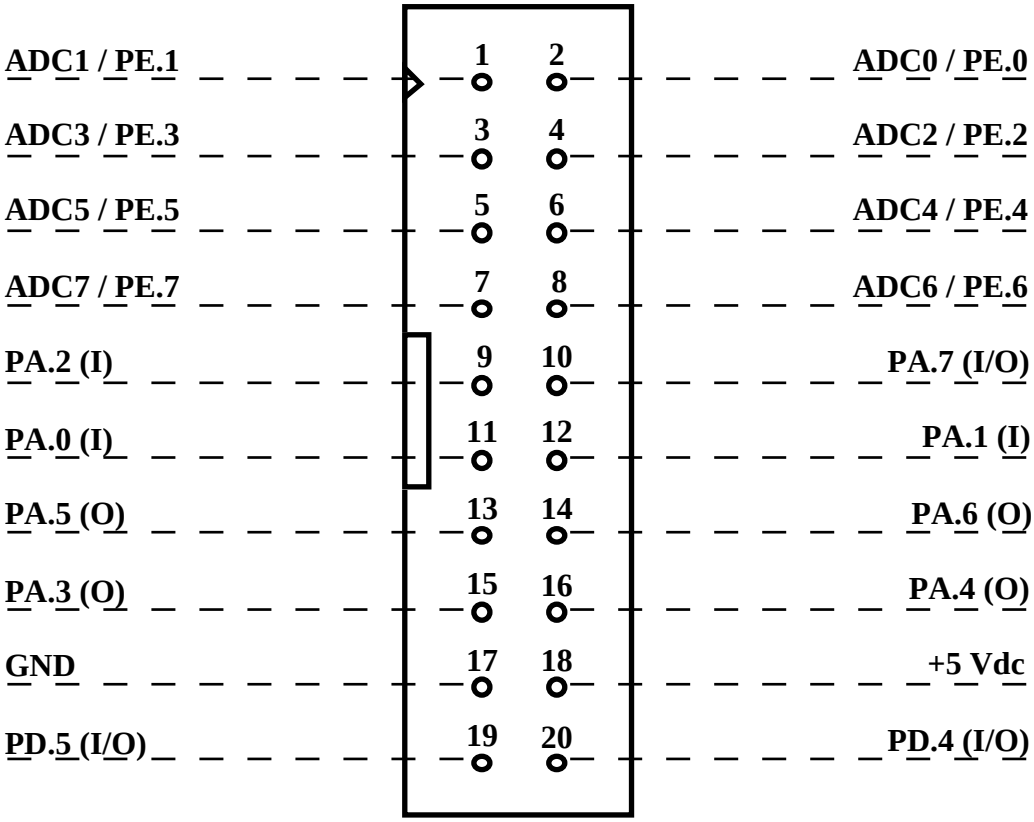


FIGURA 5: CN5 - CONNETTORE PER I/O, A/D DELLA CPU

Legenda:

PA.n	=	I/O	-	Linea digitale n del port A della CPU.
PD.n	=	I/O	-	Linea digitale n del port D della CPU.
ADCn/PE.n	=	I	-	Linea digitale n o ingresso canale n dell' A/D della CPU.
GND	=		-	Linea di massa per sezione digitale e sezione analogica.
+5 Vdc	=	O	-	Linea di alimentazione a +5 Vdc.

CN3A - CONNETTORE PER LINEA SERIALE IN RS 232

Il connettore per la comunicazione della linea seriale in RS 232 denominato CN3A sulla scheda, è del tipo PLUG a 6 vie. Le due linee di hand-shake sono simulate attraverso due pin della CPU e precisamente il CTS è controllato dal 23 (P D.3) mentre l'RTS dal pin 22 (P D.2).
La disposizione di tali segnali, riportata di seguito, è stata studiata in modo da ridurre al minimo le interferenze ed in modo da facilitare la connessione con il campo, mentre i segnali rispettano le normative definite dal CCITT relative allo standard di comunicazione usato.
Se viene acquistato il cavo CCR plug9 o 25, per compatibilità con altre schede, il 9 poli ha RTS connesso al pin 6 (DSR), il CTS é connesso al pin 4 (DTR). Il 25 poli ha RTS connesso al pin 6 (DSR), il CTS é connesso al pin 20 (DTR).

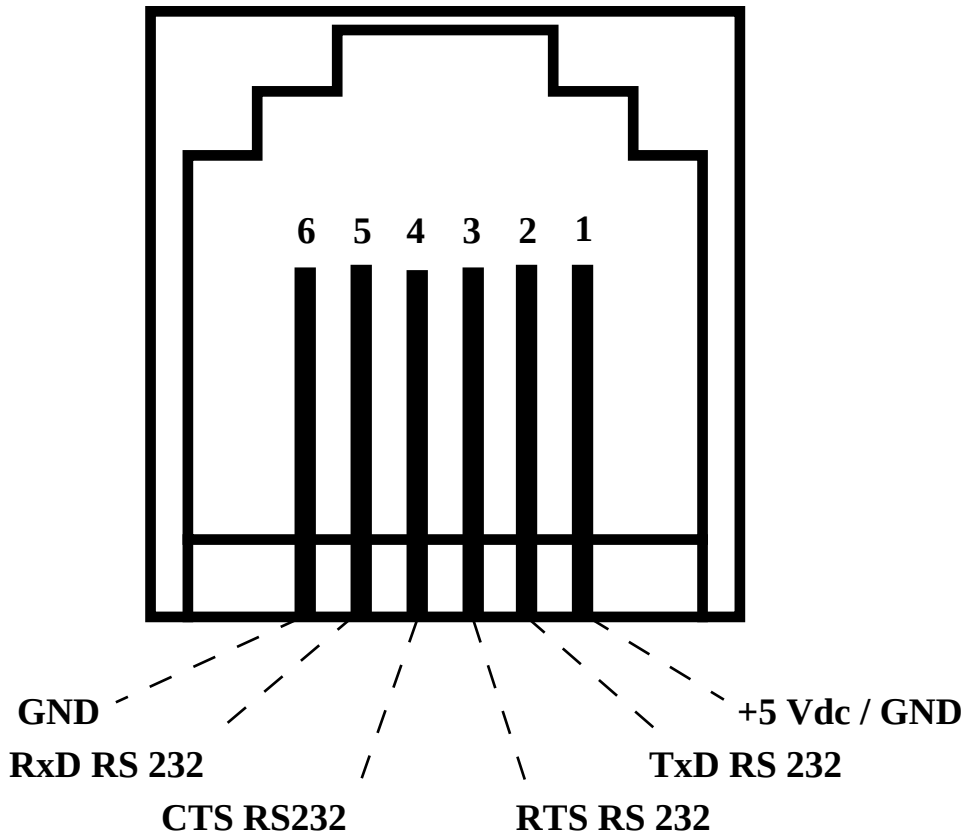


FIGURA 6: CN3A-CONNETTORE PER COMUNICAZIONE SERIALE IN RS 232

Legenda:

RxD RS 232	=	I	-	Receive Data: linea di ricezione in RS 232 della linea seriale.
TxD RS 232	=	O	-	Transmit Data: linea di trasmissione in RS 232 della linea seriale.
CTS RS 232	=	I	-	Clear To Send: linea di abilitazione della trasmissione in RS 232 della linea seriale
RTS RS 232	=	O	-	Request To Send: linea di richiesta di trasmissione in RS 232 della linea seriale
+5 Vdc/GND	=		-	Linea di alimentazione a +5 Vdc o linea di massa
GND	=			Linea di massa

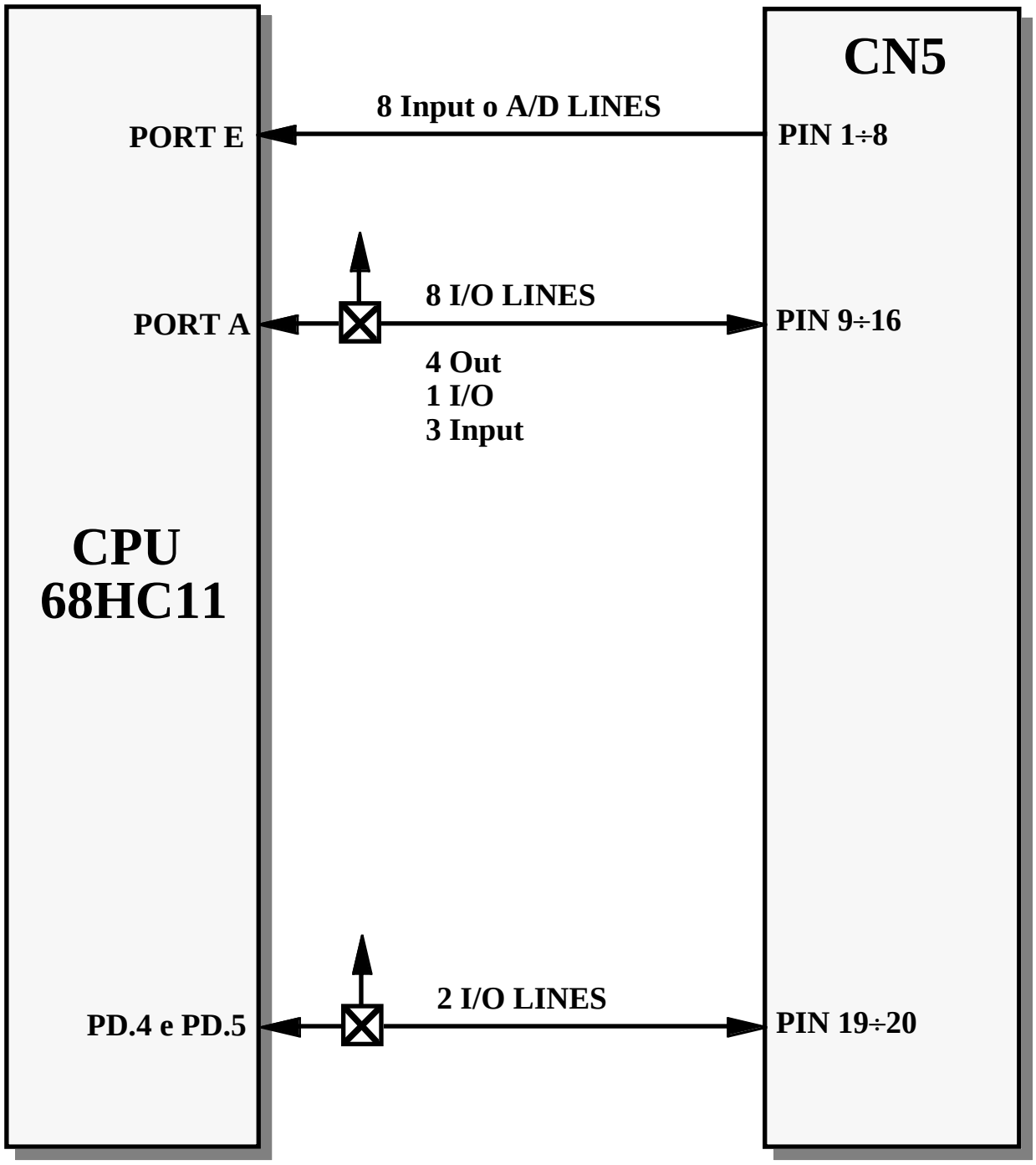


FIGURA 7: SCHEMA COLLEGAMENTO LINEE DI I/O

CN3B - CONNETTORE PER LINEA SERIALE IN RS 422-485

Il connettore per la comunicazione seriale in RS 422-485, denominato CN3B sulla scheda, è del tipo PLUG a 6 vie. La disposizione di tali segnali, riportata di seguito, è stata studiata in modo da ridurre al minimo le interferenze ed in modo da facilitare la connessione con il campo, mentre i segnali rispettano le normative definite dal CCITT relative allo standard di comunicazione usato.

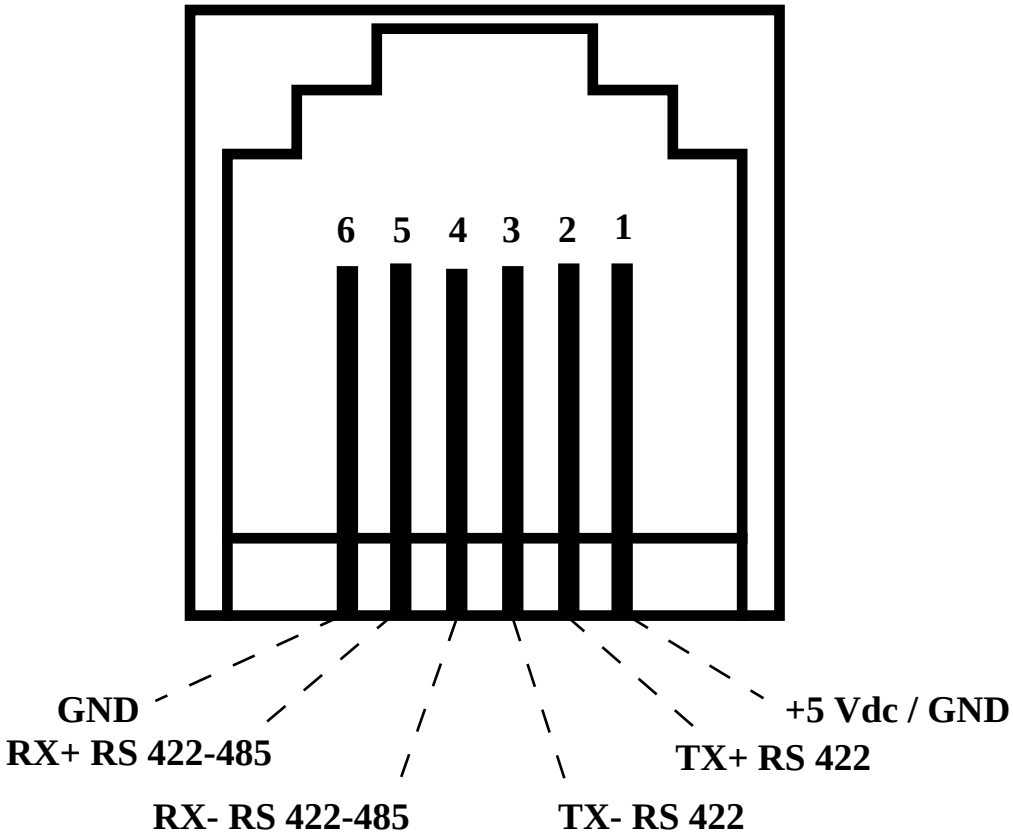


FIGURA 8: CN3B-CONNETTORE PER COMUNICAZIONE IN RS 422-485

Legenda:

RX- RS 422-485 =	I	-	Receive Data Negative: linea bipolare negativa per ricezione seriale differenziale in RS 422-485.
RX+ RS 422-485=	I	-	Receive Data Positive: linea bipolare positiva per ricezione seriale differenziale in RS 422-485.
TX- RS 422 =	O	-	Transmit Data Negative: linea bipolare negativa per trasmissione seriale differenziale in RS 422-485.
TX+ RS 422 =	O	-	Transmit Data Positive: linea bipolare positiva per trasmissione seriale differenziale in RS 422-485.
+5 Vdc/GND =		-	Linea di alimentazione a +5 Vcc o linea di massa
GND =			Linea di massa

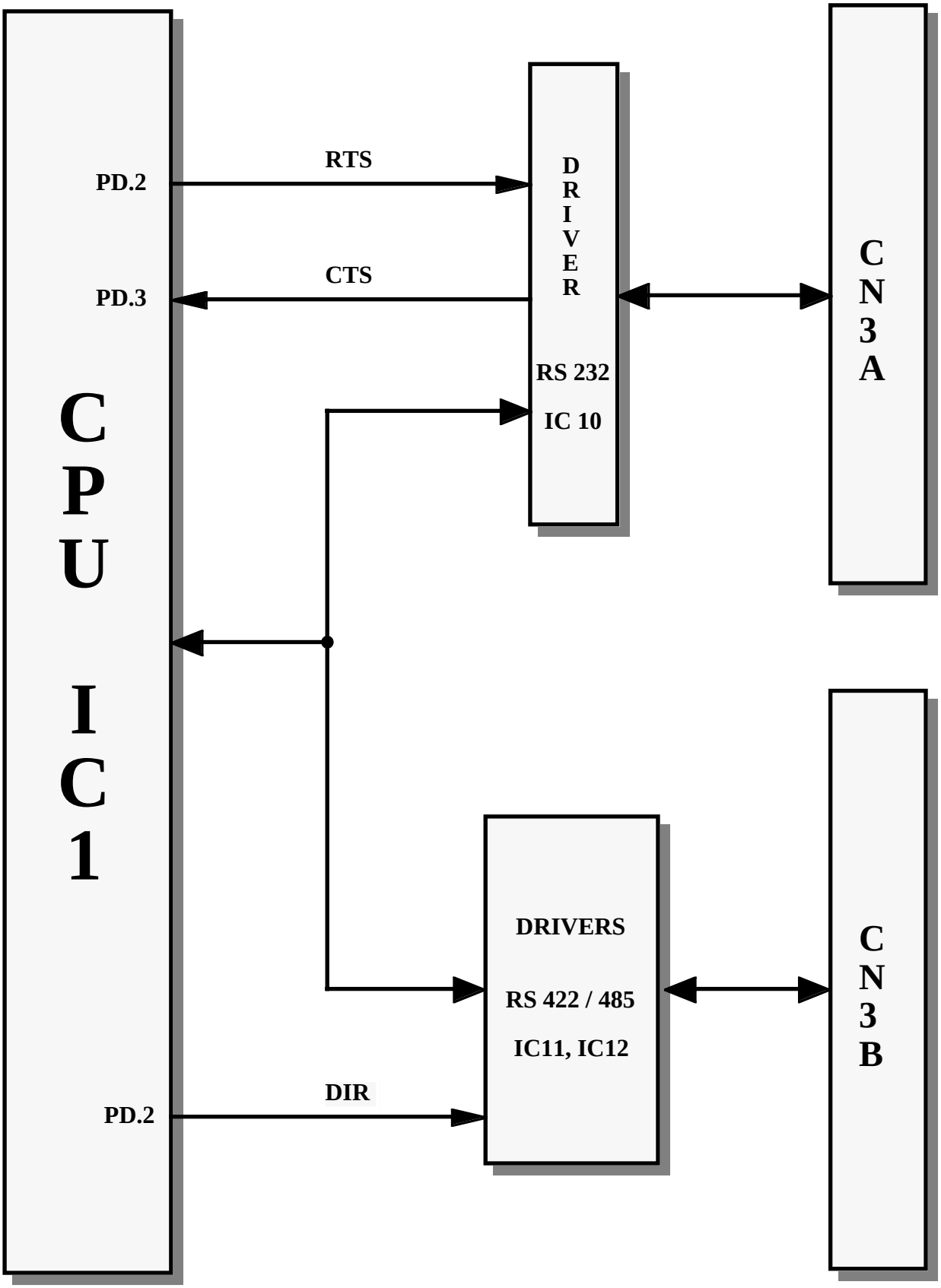


FIGURA 9: SCHEMA DI COMUNICAZIONE SERIALE

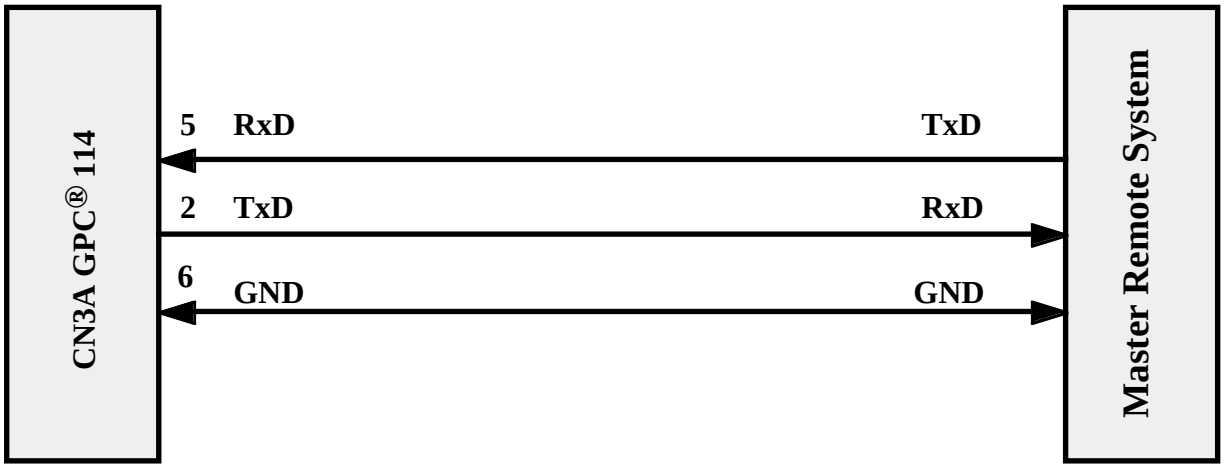


FIGURA 10: PIN-OUT PER RS 232 ED ESEMPIO DI COLLEGAMENTO

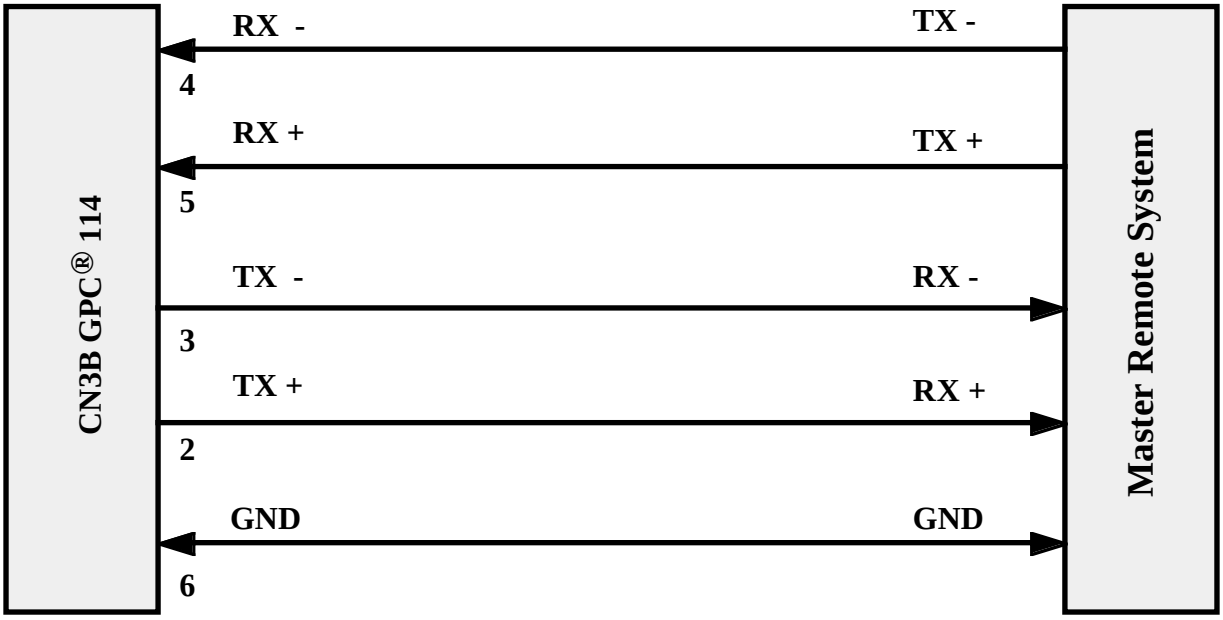


FIGURA 11: PIN-OUT PER RS 422 ED ESEMPIO DI COLLEGAMENTO

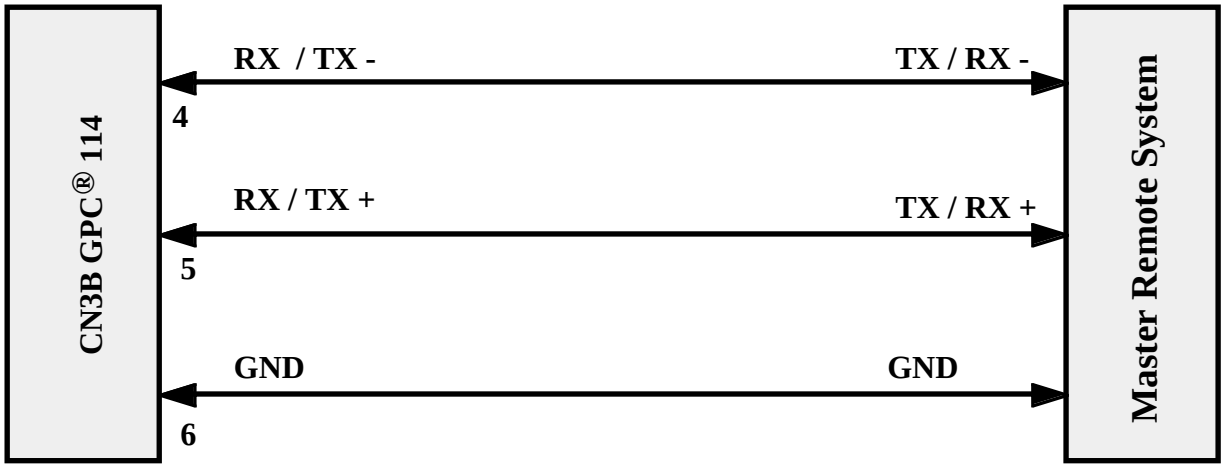


FIGURA 12: PIN-OUT PER RS 485 ED ESEMPIO DI COLLEGAMENTO

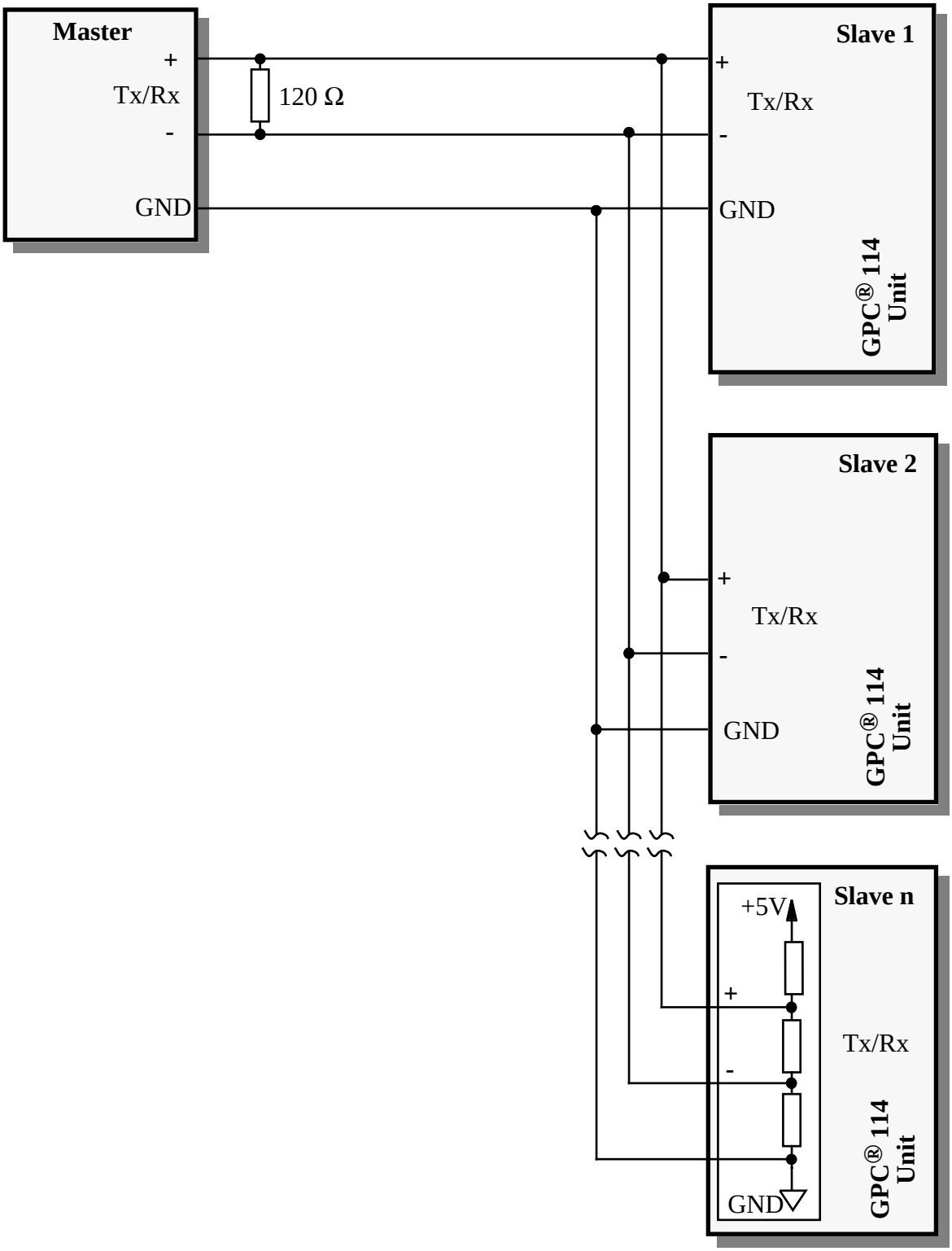


FIGURA 13: ESEMPIO DI COLLEGAMENTO IN RETE PER COMUNICAZIONE IN RS 485

INTERFACCIAMENTO DEGLI I/O CON IL CAMPO

Al fine di evitare eventuali problemi di collegamento della scheda con tutta l'elettronica del campo a cui la **GPC® 114** si deve interfacciare, si devono seguire le informazioni riportate nei precedenti paragrafi e nelle relative figure che illustrano le modalità interne di connessione.
- Per tutti i segnali che riguardano la comunicazione seriale con il protocollo RS 232, fare riferimento alle specifiche standard di questo protocollo.
- Per tutti i segnali a livello TTL possono essere collegati a linee dello stesso tipo riferite alla massa digitale della scheda. Il livello 0V corrisponde allo stato logico 0, mentre il livello 5V corrisponde allo stato logico 1.
- I segnali d'ingresso alla sezione A/D devono essere collegati a segnali analogici a bassa impedenza che rispettino il range di variazione ammesso che può essere di 2,4900 V o 5,0000V.

TRIMMER E TARATURE

Sulla **GPC® 114** é presente un trimmer da utilizzare per la taraura della scheda. In particolare con il trimmer RV1 si può fissare il valore della tensione di riferimento su cui si basa la sezione di A/D converter.
La scheda viene sottoposta ad un accurato test di collaudo che provvede a verificare la funzionalità della stessa ed allo stesso tempo a tararla in tutte le sue parti. La taratura viene effettuata in laboratorio a temperatura costante di +20 gradi centigradi, seguendo la procedura di seguito descritta:

- Si effettua la taratura di precisione della Vref della sezione A/D tramite la regolazione del trimmer RV1, tramite un multimetro galvanicamente isolato a 5 cifre ad un valore di 2,4900 V o 5,0000V.
- Si verifica la corrispondenza tra segnale analogico fornito in ingresso e combinazione letta dalla sezione A/D converter. La verifica viene effettuata fornendo un segnale di verifica con un calibratore campione e controllando che la differenza tra la combinazione determinata dalla scheda e quella determinata in modo teorico, non superi la somma degli errori della sezione A/D.
- Si blocca il trimmer della scheda, opportunamente tarato, tramite vernice.

Le sezioni d'interfaccia analogica utilizzano componenti di alta precisione che vengono addirittura scelti in fase di montaggio, proprio per evitare lunghe e complicate procedure di taratura. Per questo una volta completato il test di collaudo e quindi la taratura, il trimmer RV1 viene bloccato, in modo da garantire una immunità della taratura anche ad eventuali sollecitazioni meccaniche (vibrazioni, spostamenti, ecc.).
La circuiteria di generazione della tensione di riferimento definisce anche il fondo scala per tutti gli 8 canali di ingresso analogico, tra i due possibili range: 0÷2,49 V o 0÷5,00 V. La scelta di questo valore di fondo scala deve essere specificata in fase d'ordine della scheda, infatti implica il montaggio di diversi componenti ed una diversa procedura di taratura. In assenza di indicazioni, la scheda viene fornita nella versione standard con fondo scala a 2,49 V.
L'utente di norma non deve intervenire sulla taratura della scheda, ma se lo dovesse fare (a causa di derive termiche, derive del tempo, ecc.) deve rigorosamente seguire la procedura sopra illustrata.
Per una facile individuazione del trimmer a bordo scheda, si faccia riferimento alla figura 19.

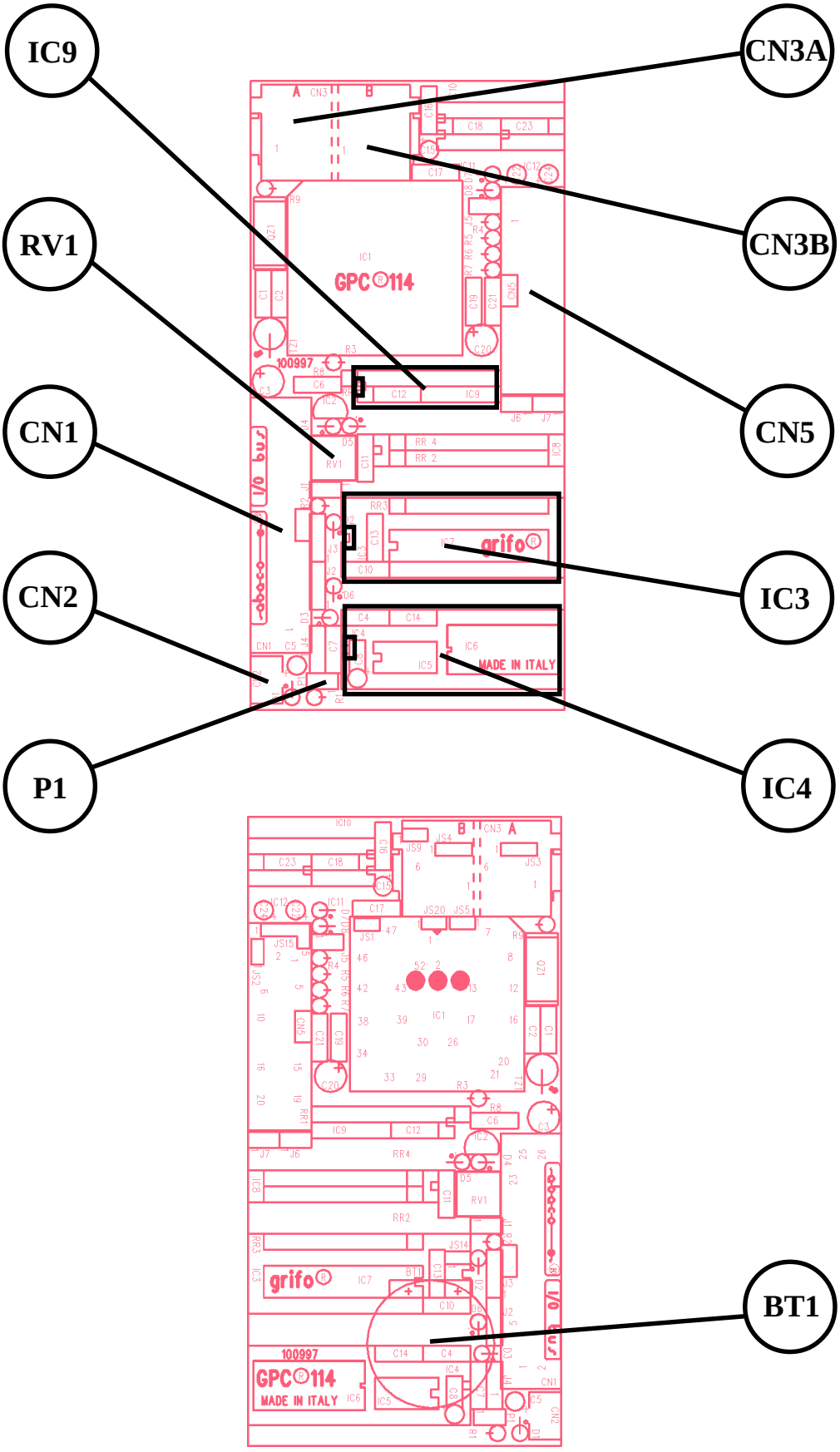


FIGURA 14: DISPOSIZIONE P1, CONNETTORI, RV1, BT1 E MEMORIE .

JUMPERS

Esistono a bordo della **GPC® 114** 16 jumpers, con cui è possibile effettuare alcune selezioni che riguardano il modo di funzionamento della stessa. Di seguito ne è riportato l'elenco, l'ubicazione e la loro funzione nelle varie modalità di connessione.

JUMPERS	N. VIE	UTILIZZO
J1	2	Collega il pin 1 di IC9 (RTC) alla linea di inerrupt /IRQ della CPU.
J2	3	Seleziona il size e il dispositivo di memoria su IC 4.
J3	3	Seleziona il dispositivo di memoria su IC 4.
J4	3	Seleziona il dispositivo di memoria su IC 4.
J5	2	Ingresso utente (RUB/DEBUG).
J6, J7	2	Seleziona la mappa di memoria.
JS1, JS2	2	Collegano la circuiteria di terminazione e forzatura alla linea di comunicazione seriale in RS 422-485.
JS3	3	Seleziona il tipo di collegamento per il pin 1 di CN3A.
JS4	3	Seleziona il tipo di collegamento per il pin 1 di CN3B.
JS9	2	Riservato .
JS14	2	Collega la batteria di bordo BT1 alla circuiteria di back-up.
JS15	5	Seleziona direzionalità e modalità di attivazione della linea seriale in RS 422-485.
JS5, JS20	2	Selezionano il modo operativo della CPU.

FIGURA 15: TABELLA RIASSUNTIVA JUMPERS

Di seguito è riportata una descrizione tabellare delle possibili connessioni dei 16 jumpers con la loro relativa funzione. Per riconoscere tali connessioni sulla scheda si faccia riferimento alla serigrafia della stessa o alla figura 2 di questo manuale, dove viene riportata la numerazione dei pins dei jumpers, che coincide con quella utilizzata nella seguente descrizione. Per l'individuazione dei jumpers a bordo della scheda, si utilizzi invece la figura 25.

JUMPERS A 2 VIE

Per il corretto utilizzo dei jumpers JS5 e JS20, è necessario consultare il manuale tecnico del microcontrollore, dove vengono illustrate le quattro modalità operative che esso sopporta, tenendo presente che JS20, quando è connesso, setta il pin 2 (MODB) della CPU a "0", mentre JS5, quando è connesso, setta il pin 3 (MODA) della CPU a "0".

JUMPERS	CONNESSIONE	UTILIZZO	DEF.
J1	non connesso	Non collega il segnale STD (pin 1) dell'RTC IC9, alla linea di /IRQ della CPU IC1.	*
	connesso	Collega il segnale STD (pin 1) dell'RTC IC9, alla linea di /IRQ della CPU IC1.	
JS1, JS2	non connessi	Non collegano la circuiteria di terminazione e di forzatura alla linea di comunicazione della seriale in RS 422-485.	*
	connessi	Collegano la circuiteria di terminazione e di forzatura alla linea di comunicazione della seriale in RS 422-485.	
JS5	non connessi	MODA:seleziona un livello logico "1" (pin3).	*
	connessi	MODA:seleziona un livello logico "0" (pin3).	
JS9	connesso	Riservato.	*
JS14	non connesso	Non collega la batteria di bordo BT1 alla circuiteria di back-up.	*
	connesso	Collega la batteria di bordo BT1 alla circuiteria di back-up.	
JS20	non connessi	MODB: seleziona un livello logico "1" (pin2).	*
	connessi	MODB: seleziona un livello logico "0" (pin2).	

FIGURA 16: TABELLA JUMPERS A 2 VIE

L' * indica la connessione di default, ovvero la connessione impostata in fase di collaudo, con cui la scheda viene fornita.
Se si connette il jumper JS5, con una pallina di stagno, alla prossima accensione verrà lanciato automaticamente il monitor debugger ROM BUFFALO che si trova all'interno del 68HC11A1, per utilizarlo basta connettersi sulla seriale RS232 a 9600 baud (CPU a 8MHz), tramite un programma di comunicazione ad esempio il GET11, disponibile anche in web.

JUMPERS A 3 VIE

JUMPERS	CONNESSIONE	UTILIZZO	DEF.
J2	posizione 1-2	Predispone IC4 per RAM/EEPROM/EPROM da 32 K.	*
	posizione 2-3	Predispone IC4 per RAM/EEPROM da 8 K.	
	Non connesso	Predispone IC4 per EPROM da 8 K.	
J3	posizione 1-2	Predispone IC4 per EPROM	
	posizione 2-3	Predispone IC4 per RAM/EEPROM da 32 K.	*
	Non connesso	Predispone IC4 per RAM/EEPROM da 8 K.	
J4	posizione 1-2	Predispone IC4 per EPROM.	
	posizione 2-3	Predispone IC4 per RAM/EEPROM.	*
JS3	posizione 1-2	Collega il pin 1 di CN3A a GND.	*
	posizione 2-3	Collega il pin 1 di CN3A a +5 Vcc.	
JS4	posizione 1-2	Collega il pin 1 di CN3B a GND.	*
	posizione 2-3	Collega il pin 1 di CN3B a +5 Vcc.	

FIGURA 17: TABELLA JUMPERS A 3 VIE

L' * indica la connessione di default, ovvero la connessione impostata in fase di collaudo, con cui la scheda viene fornita.

JUMPER A 5 VIE

JUMPERS	CONNESSIONE	UTILIZZO	DEF.
JS15	posizione 1-2 e 3-4	Seleziona comunicazione su linea seriale in RS 485 (half duplex a 2 fili)	
	posizione 2-3 e 4-5	Seleziona comunicazione su linea seriale in RS 422-485 (full duplex o half duplex a 4 fili)	

FIGURA 18: TABELLA JUMPER A 5 VIE

L' * indica la connessione di default, ovvero la connessione impostata in fase di collaudo, con cui la scheda viene fornita.

NOTE

Vengono di seguito riportate una serie di indicazioni con cui descrivere in modo più dettagliato quali sono le operazioni da eseguire per configurare correttamente la scheda.

GESTIONE INTERRUPTS

Una caratteristica peculiare della **GPC® 114** è la notevole potenza nella gestione delle interruzioni. Di seguito viene riportata una breve descrizione di come possono essere gestiti i segnali hardware di interrupt della scheda; per quanto riguarda la gestione di tali interrupts si faccia riferimento ai data sheets del microprocessore.

/INT **RTC** tramite STD (J1) -> genera un segnale di interrupt sul pin 19 (/IRQ) della CPU.
/INT **ABACO®** I/O BUS -> genera un segnale di interrupt sul pin 19 (/IRQ) della CPU.
/NMI **ABACO®** I/O BUS -> genera un segnale di interrupt sul pin 18 (XIRQ) della CPU.

Alle risorse sopra descritte vanno naturalmente aggiunte tutte le sezioni interne al microprocessore, che possono a loro volta generare interrupts.

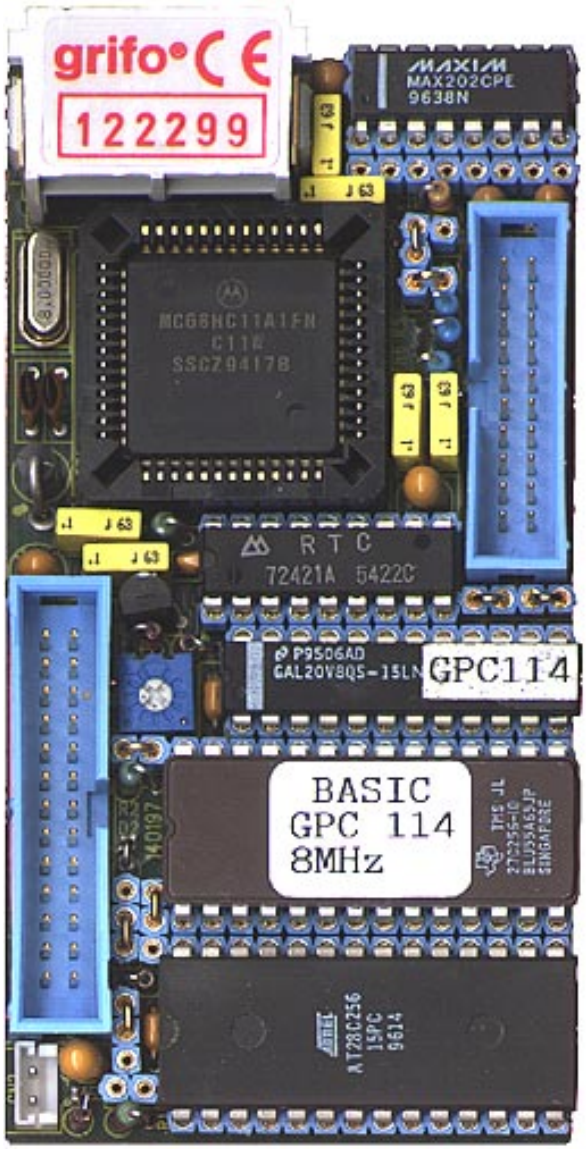


FIGURA 19: FOTO DELLA SCHEDA

SELEZIONE DEL TIPO DI COMUNICAZIONE SERIALE

La linea di comunicazione seriale della scheda **GPC® 114** può essere bufferata in RS 232 o in RS 422-485. La selezione del tipo d'interfacciamento avviene via hardware e viene effettuata tramite un opportuno strippaggio dei jumpers di bordo, come può essere desunto dalla lettura delle precedenti tabelle. Dal punto di vista software sono invece definibili tutti i parametri del protocollo fisico di comunicazione tramite la programmazione dei registri interni della CPU. Vengono di seguito riportate le possibili configurazioni che possono essere effettuate; da notare che i jumpers non menzionati nella sucessiva descrizione, non hanno alcuna influenza ai fini della comunicazione, qualunque posizione essi occupino.

- LINEA SERIALE SETTATA IN RS 232
  Su IC10 deve essere montato il driver MAX 232 mentre su IC11, IC12, non deve essere montato nessun driver.

- LINEA SERIALE SETTATA IN RS 485
  Su IC 12 deve essere montato il driver SN75176 mentre su IC 10 non deve essere montato nessun driver. Il jumper J5 deve essere in posizione 2-3 e 4-5. In questa modalità le linee da utilizzare sono i pin 4 e 5 di CN3B, che quindi diventano le linee di trasmissione o ricezione a seconda dello stato del segnale DIR gestito via software. Questa comunicazione la si utilizza per comunicazioni su sistemi multipunto, infatti il driver su IC 12 può essere settato in ricezione o in trasmissione, tramite la gestione del segnale DIR (0=basso= ricezione, 1=alto=trasmissione). Sempre in questa modalità è possibile ricevere quanto trasmesso, in modo da fornire al sistema la possibilità di verificare autonomamente la riuscita della trasmissione, infatti in caso di conflitti sulla linea, quanto trasmesso non viene ricevuto correttamente e viceversa.

- LINEA SERIALE SETTATA IN RS 422
  Su IC 11 e IC 12 devono essere montati i drivers SN75176 mentre su IC 10, non deve essere montato nessun driver. Il jumper J5 deve essere in posizione 1-2 e 3-4. Per sistemi punto punto, la linea DIR può essere mantenuta sempre alta (trasmettitore sempre attivo), mentre per sistemi multipunto si deve attivare il trasmettitore solo in corrispondenza della trasmissione sempre tramite la linea DIR (1=alto=trasmettitore attivo e viceversa).

Nel caso si utilizzi la linea seriale in RS 422-485, con i jumpers JS1 e JS2 è possibile connettere la circuiteria di terminazione e forzatura sulla linea . Tale circuiteria deve essere sempre presente nel caso di sistemi punto punto, mentre nel caso di sistemi multipunto, deve essere collegata solo sulle schede che risultano essere alla maggior distanza, ovvero ai capi della linea di comunicazione.
Per una facile individuazione dei jumpers e dei driver seriali fare riferimento all'appendice A.

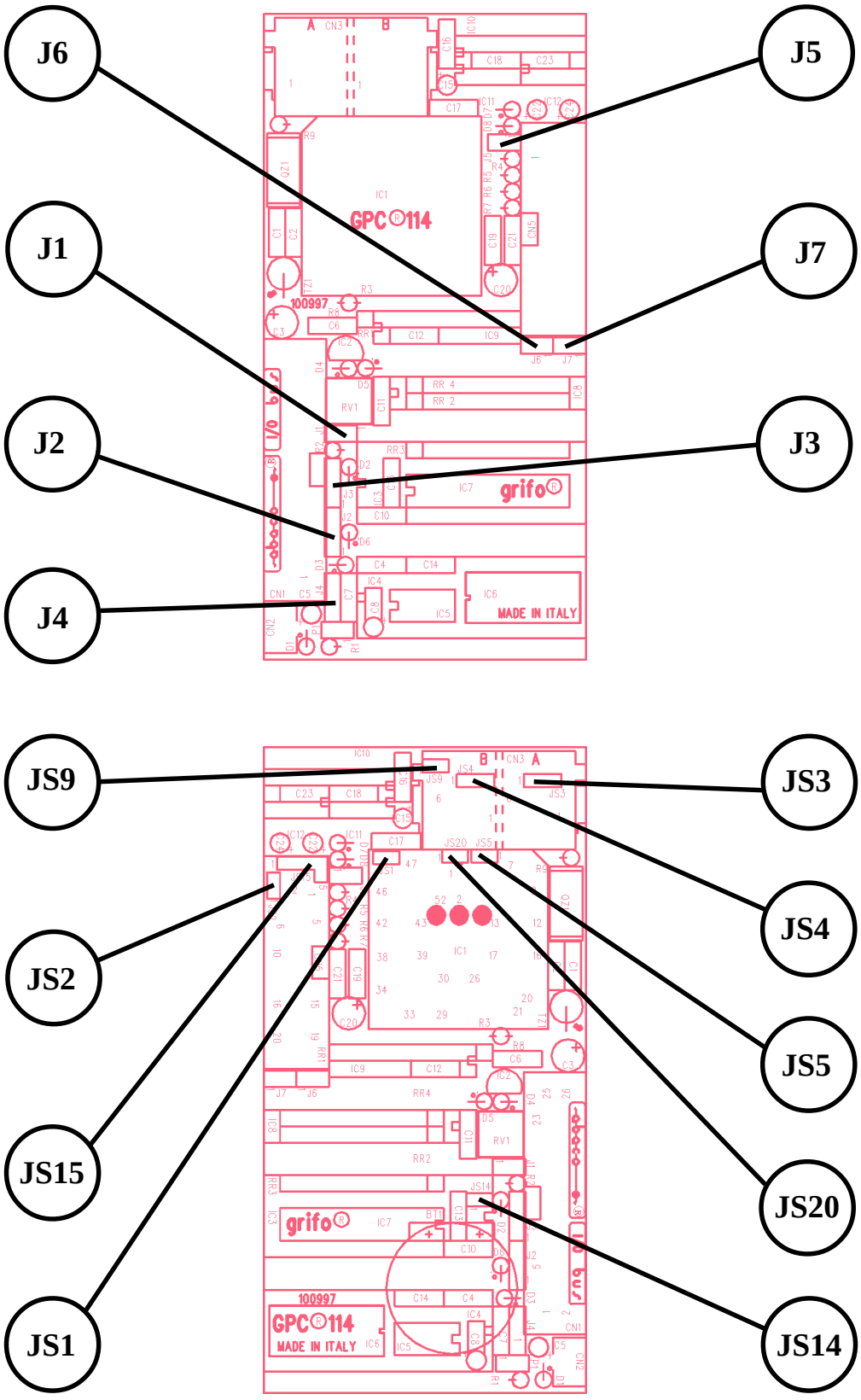


FIGURA 20: DISPOSIZIONE JUMPERS LATO COMPONENTI E LATO STAGNATURA

SELEZIONE MEMORIE

La **GPC® 114** può montare fino ad un massimo di 64K bytes di memoria variamente suddivisa. In particolare valgono le informazioni riportate nella seguente tabella:

IC	DISPOSITIVO	DIMENSIONE	STRIPPAGGIO
4	RAM/EEPROM	8K Bytes	J2 in 2-3; J3 non connesso; J4 in 2-3
	RAM/EEPROM	32K Bytes	J2 in 1-2; J3 in 2-3; J4 in 2-3
	EPROM	8K Bytes	J2 non connesso; J3 in 1-2; J4 in 1-2
	EPROM	32K Bytes	J2 in 1-2; JJ3 in 1-2; 4 in 1-2
6	RAM	32K Bytes	
3	EPROM	32K Bytes	

FIGURA 21: TABELLA DI SELEZIONE MEMORIE

Per quanto riguarda le sigle dei vari dispositivi che possono essere montati, fare riferimento alla documentazione della casa costruttrice. I moduli di RAM per IC 4, possono, su richiesta, essere del tipo tamponato.

BACK UP

La **GPC® 114** é provvista di una batteria al litio BT1 che provvede a tamponare la RAM ed il RTC di bordo anche in assenza della tensione di alimentazione. Il jumper JS14 provvede al collegamento di questa batteria in modo da salvaguardarne la durata prima dell'installazione o in tutti i casi in cui il back up non é necessario. Una seconda batteria esterna può essere collegata alla circuiteria di back up tramite il connettore CN2: quest'ultima non é interessata dalla configurazione del jumper JS14 e sostituisce a tutti gli effetti la BT1.
Per la scelta della batteria esterna di back up seguire le indicazioni del paragrafo "CARATTERISTICHE ELETTRICHE", mentre per la sua individuazione si veda la figura 19.

DESCRIZIONE SOFTWARE

Questa scheda ha la possibilita' di usufruire di una ricca serie di strutture software che consentono di utilizzarne al meglio le caratteristiche. In generale la scheda puo' sfruttare tutte le risorse software disponibili per il processore montato, ovvero i numerosi pacchetti ideatiper il 68HC11. Tra questi ricordiamo:

KERNEL: Sistema con cui sviluppare procedure di controllo in real time e sistemi di acquisizione dati. Il pacchetto risiede in EPROM, mentre l'applicativo realizzato puo' risiedere sia in RAM (fase di debug), che in EPROM (fase definitiva). Opera in congiunzione con un programma di interfaccia utente che opera su un Personal Computer esterno, collegato in RS 232. Il pacchetto è dotato di funzioni di libreria di normale utilizzo.

BUFFALO: Monitor Debugger in grado di lavorare in tutti i modi operativi del 68HC11 e di debuggare qualsiasi programma sviluppato per questo microprocessore. In congiunzione con un normale P. C. si ha a disposizione lo stato completo della scheda, analogamente a quanto disponibile con un emulatore. Il pacchetto software dispone dei comandi generici di esame e modifica della memoria, programmazione e lettura dell'EEPROM, caricamento ed esecuzione codice, ecc.
(Mappa 1)

ROM BUFFALO: Ha le stesse caratteristiche del Buffalo é disponibile nel processore 68HC11A1, infatti si trova nella ROM interna del microcontrollore e si attiva modificando il il modo operativo agendo sui jumper JS5 e JS20, per chiarimenti vedere figura 21 e figura 25.

CONTROL PASCAL: Sistema di programmazione che utilizza un sottoinsieme delle istruzioni PASCAL, in grado di generare un codice direttamente eseguibile sulla **GPC® 114**. Il pacchetto è composto da una serie di programmi eseguibili su un P.C. con cui è possibile editare, tradurre e compilare l'applicativo realizzato. Quindi il codice ottenuto puo' essere eseguito direttamente sulla scheda la quale è in esecuzione di un programma interattivo fornito in EPROM, provvisto del modulo di run time. (Mappa 4)

C I.A.S.: Pacchetto software in grado di eseguire il codice sviluppato da un programma scritto in C. Il pacchetto è composto da una serie di programmi eseguibili su un P.C. con cui è possibile editare, tradurre e compilare l'applicativo realizzato. Quindi il codice ottenuto puo' essere eseguito direttamente sulla scheda la quale è in esecuzione di un programma interattivo fornito in EPROM, provvisto del modulo di run time. Assieme al pacchetto software sono disponibili anche tutte le funzioni di libreria che consentono di sfruttare le risorse della **GPC® 114**.

BASIC 11:È una completa struttura di sviluppo che consente di programmare la scheda con un BASIC interpretato adatto alle applicazioni industriali. Per opearare è sufficiente un P.C. che svolge le funzioni di consolle nei confronti della scheda su cui viene invece sviluppato, debuggato, provato e salvato il programma da realizzare. La programmazione è ad alto livello ed interessa la maggioranza dei dispositivi a bordo scheda di cui vengono già forniti i driver software di facile utilizzo.
(Mappa 1)

HI-TECH C: Cross compilatore per file sorgenti scritti in linguaggio "C". È un potente pacchetto software che tramite un comodo I.D.E. permette di utilizzare un editor, un compilatore "C" (floating-point), un assemblatore, un linker e un remote debugger. Sono inoltre inclusi i source delle librerie.
(Mappa 4)
ICC11: Cross compilatore per file sorgenti scritti in linguaggio "C" in ambiente Windows. È un potente pacchetto software che tramite un comodo I.D.E. permette di utilizzare un editor, un compilatore "C" (floating-point), un assemblatore, un linker ed in abbinamento al NOICE11 un remote debugger. Sono inoltre inclusi i source delle librerie. (Mappa 4)
NOICE11: Monitor Debugger in grado debuggare qualsiasi programma sviluppato per questo microprocessore. In congiunzione con un normale P. C. si ha a disposizione lo stato completo della scheda, analogamente a quanto disponibile con un emulatore. Il pacchetto software dispone dei comandi generici di esame e modifica della memoria, programmazione, caricamento ed esecuzione codice, ecc. Se viene abbinato al pacchetti ICC11, é possibile eseguire il debugger riga per riga con il sorgente "C" a video. (Mappa 1)
DDS C: È un comodo pacchetto software, a basso costo, che tramite un completo I.D.E. permette di utilizzare un editor, un compilatore "C" (integer), un assemblatore, un linker e un remote debugger abbinato ad un monitor. Sono inclusi i sorgenti delle librerie ed una serie di utility. (Mappa 4)

MAPPAGGI ED INDIRIZZAMENTI

INTRODUZIONE

In questo capitolo ci occuperemo di fornire tutte le informazioni relative all'utilizzo della scheda, dal punto di vista della programmazione via software. Tra queste si trovano le informazioni riguardanti il mappaggio della scheda e la gestione software delle sezioni componenti.

MAPPAGGIO DELLE RISORSE DI BORDO

La gestione delle risorse della scheda è affidata ad una logica di controllo completamente realizzata con logiche programmabili. Essa si occupa del mappaggio delle zone di RAM ed EPROM e di tutte le periferiche di bordo, semplificando l' operatività dell' utente. La logica di controllo è realizzata in modo da gestire separatamente il mappaggio delle memorie di bordo ed il mappaggio delle periferiche viste in Input/Output. Tale logica di controllo è realizzata in modo da allocare tutti i dispositivi di bordo all'interno dello spazio d'indirizzamento massimo di 64 KByte. Questa gestione è effettuata via hardware tramite lo strippaggio di alcuni jumpers (J2, J3, J4, J6, J7) con cui si può definire quali memorie utilizzare e il range di indirizzamento per ciascuna di esse.
Riassumendo i dispositivi mappati sulla scheda sono essenzialmente:

- 32K Bytes di EPROM su IC 3
- 32K Bytes di RAM su IC 6 saldati
- Fino a 32K Bytes di RAM/EEPROM/EPROM su IC 8
- **Abaco® I/O BUS**
- RTC 72421 IC9 (RUN/DEBUG stato di J5).

Questi occupano gli indirizzi riportati nei paragrafi seguenti e non possono essere riallocati in nessun altro indirizzo, per una facile individuazione dei dispositivi vedi figura 14.

MAPPAGGIO DELL'I/O

Per quanto riguarda l' I/O sono state riservate delle aree di memoria per un totale di 256 indirizzi (128 utilizzati per l' **Abaco® I/O BUS**, 32 bytes per l'RTC e 32 bytes per il chip enable ECS1) dei 64K bytes dell' area dati gestita dalla CPU. Per maggior chiarezza si riporta il nome del registro, il suo indirizzo, il tipo di accesso ed una breve descrizione del loro significato:

DISP.	REG.	IND.	R/W	SIGNIFICATO
Abaco® I/O BUS	/ECS1	B800H÷B83FH	R/W	Indirizzi I/O BUS, mappa 1,2,3 .
	I/O BUS	B840H÷B8BFH	R/W	
RTC IC9 , J5	16 Reg.	B8C0H÷B8FFH	R/W	Reg. per la gestione del dispositivo, mappa 1,2,3 .
Abaco® I/O BUS	/ECS1	7F00H÷7F3FH	R/W	Indirizzi I/O BUS, mappa 4 .
	I/O BUS	7F40H÷7FBFH	R/W	
RTC IC9 , J5	16 Reg.	7FC0H÷7FFFH	R/W	Reg. per la gestione del dispositivo, mappa 4 .

FIGURA 22: TABELLA INDIRIZZAMENTO I/O

Per quanto riguarda la descrizione del significato dei registri qui sopra riportati, si faccia riferimento al capitolo sucessivo "DESCRIZIONE SOFTWARE DELLE PERIFERICHE DI BORDO".

MAPPAGGIO DELLE MEMORIE

Per quanto riguarda il mappaggio delle memorie, la scheda può essere configurata in 4 modi. Di seguito viene riportata una schematizzazione di questi indirizzamenti, con le indicazioni di come devono essere strippati i jumpers J6 e J7 che svolgono questa selezione, le zone di indirizzamento non usate, è consigliabile sfruttarle per posizionare i registri del processore, questo é possiibile farlo durante i primi 64 cicli di clok. Si ricorda che la combinazione binaria dei jumpers J6 e J7 indica il numero del mappaggio.

MAPPAGGIO 1

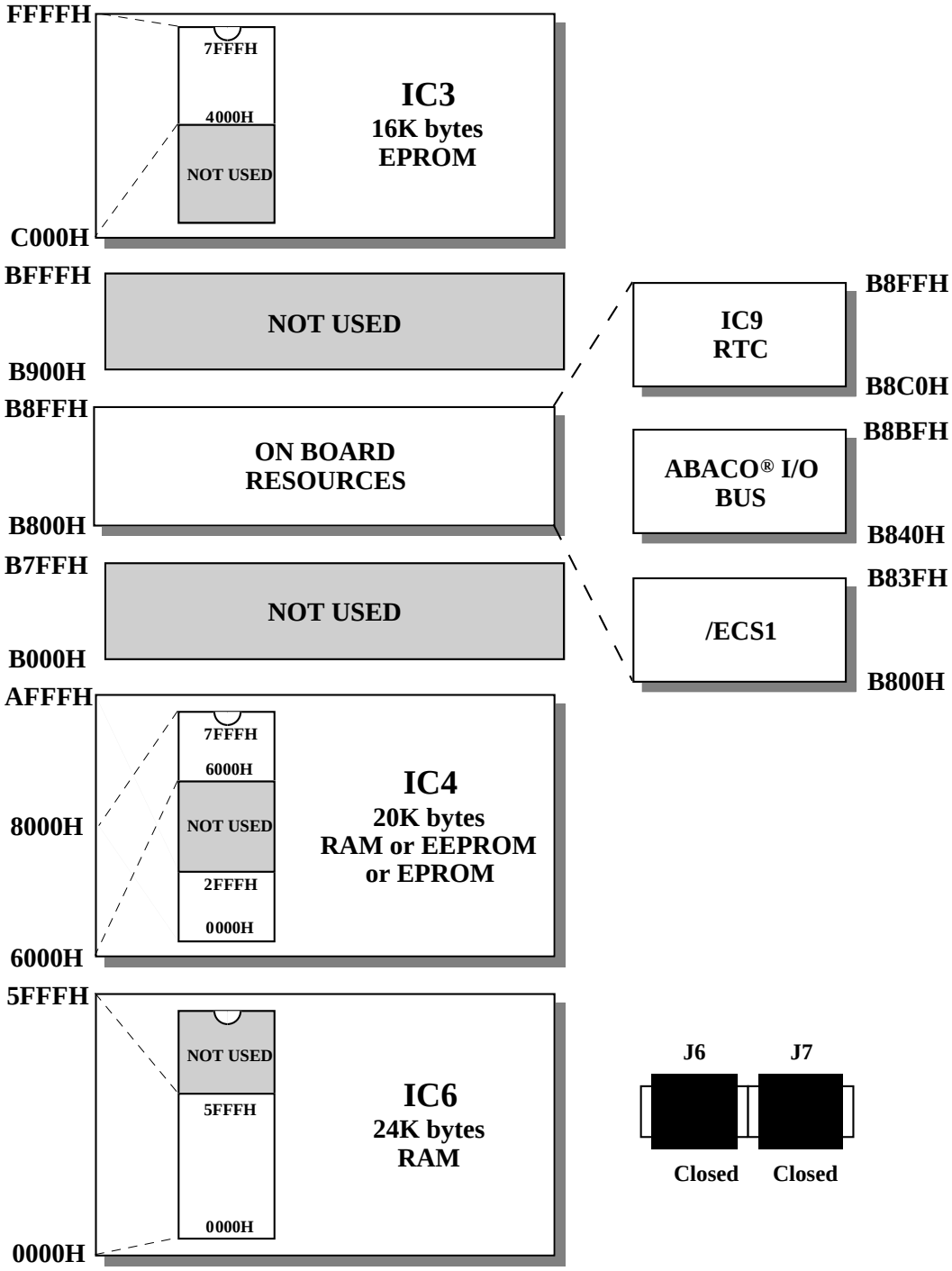


FIGURA 23: MAPPAGGIO DELLE MEMORIE IN MODO 1

Configurazione jumpers: J6 in posizione **CONNESSO; J7** in posizione **CONNESSO**

MAPPAGGIO 2

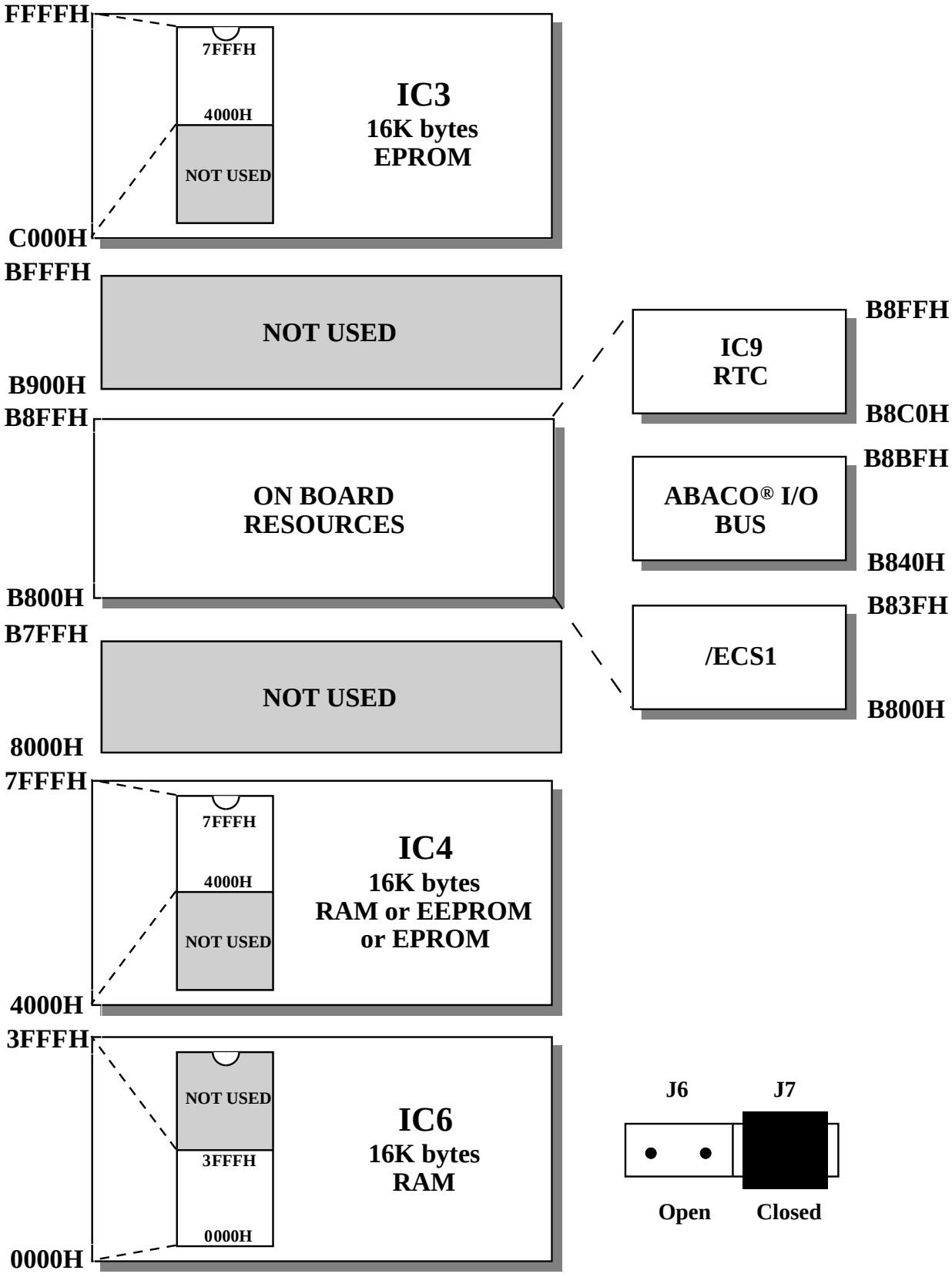


FIGURA 24: MAPPAGGIO DELLE MEMORIE IN MODO 2

Configurazione jumpers: J6 in posizione **NON CONNESSO; J7** in posizione **CONNESSO**

MAPPAGGIO 3

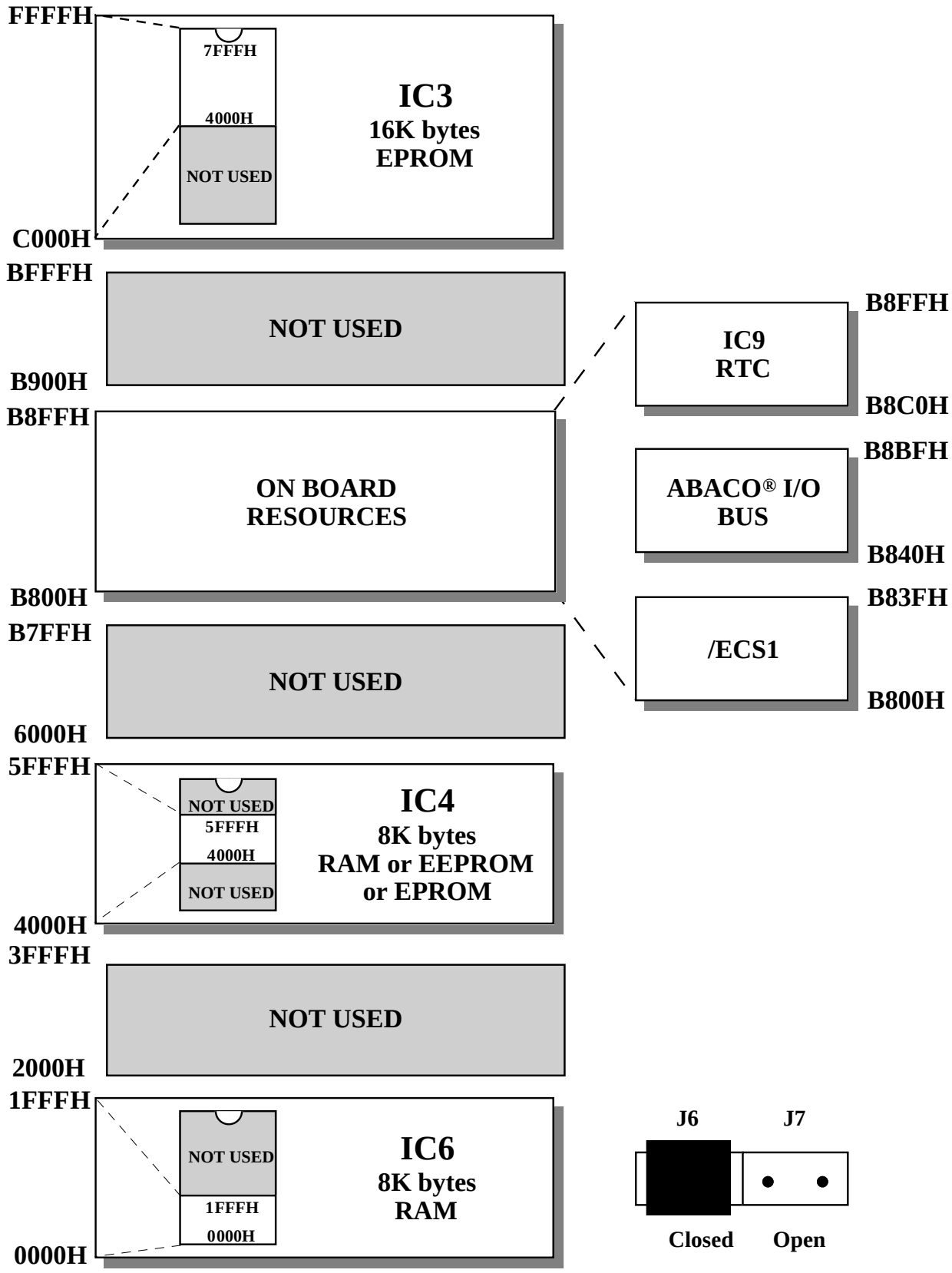


FIGURA 25: MAPPAGGIO DELLE MEMORIE IN MODO 3

Configurazione jumpers: J6 in posizione **CONNESSO; J7** in posizione **NON CONNESSO**

MAPPAGGIO 4

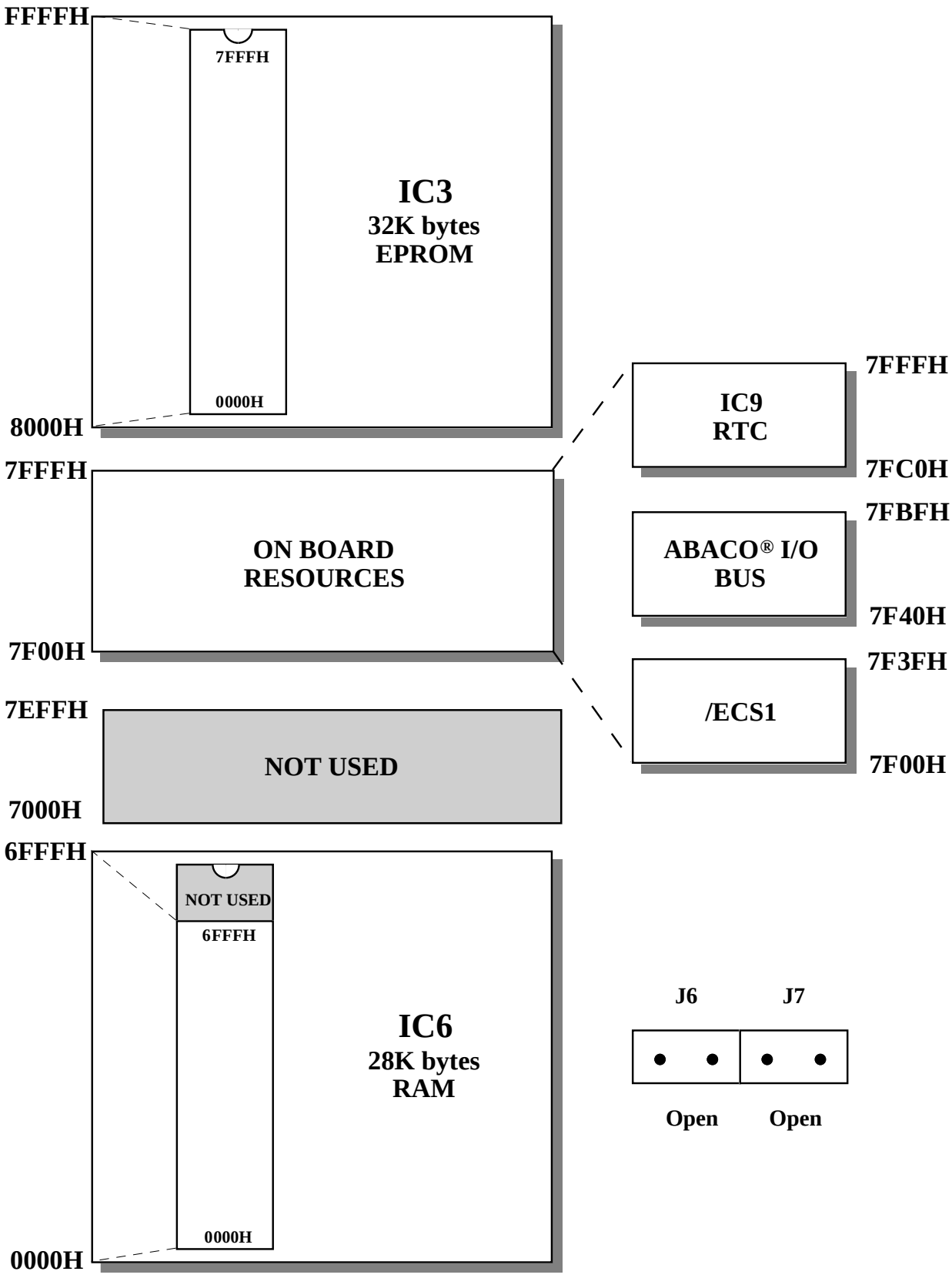


FIGURA 26: MAPPAGGIO DELLE MEMORIE IN MODO 4

Configurazione jumpers: J6 in posizione **NON CONNESSO; J7** in posizione **NON CONNESSO**

DESCRIZIONE SOFTWARE DELLE PERIFERICHE DI BORDO

Nel paragrafo precedente sono stati riportati gli indirizzi di allocazione di tutte le periferiche e di seguito viene riportata una descrizione dettagliata della funzione e del significato dei relativi registri (al fine di comprendere le sucessive informazioni, fare sempre riferimento alla tabella di indirizzamento I/O). Qualora la documentazione riportata fosse insufficiente fare riferimento direttamente alla documentazione tecnica della casa costruttrice del componente. In questo capitolo inoltre non vengono descritte le sezioni che fanno parte del microprocessore; per quanto riguarda la programmazione di quest'ultime si faccia riferimento alla documentazione tecnica della casa costruttrice del componente.

JUMPER J5 CONFIGURAZIONE INPUT UTENTE

Il jumper di configurazione J5 presente sulla **GPC® 114** può essere acquisito via software, effettuando una semplice operazione di input all'indirizzo di allocazione di uno dei 16 registri **RTC** ed esaminando il bit D7. L'acquisizione è in logica negata, ovvero il jumper connesso fornisce lo stato logico 0 al corrispondente bit, mentre il jumper non connesso fornisce lo stato logico 1.
Tale jumper svolge la funzione di selettore delle modalità RUN (non connesso) o DEBUG (connesso), caratteristica di alcuni pacchetti software della **grifo®**.

RTC 72421

Questa periferica è vista in 16 consecutive locazioni di I/O (in realtà ne vnegono attribuiti 32, ma sono soltanto duplicati) di cui 3 di stato ed i rimanenti 13 per i dati. I registri dati sono utilizzati sia per operazioni di lettura (dell' orario attuale) che di scrittura (per l' inizializzazione dell' orologio) cosi' come i registri di stato i quali sono utilizzati in scrittura (per la programmazione del modo di funzionamento dell' orologio) ed in lettura (per determinare lo stato dell' orologio). Per quanto riguarda i registri dati vale la corrispondenza:

S1	- Unita' dei secondi	- 4 bit meno significativi S1(3-0)
S10	- Decine dei secondi	- 3 bit meno significativi S10(2-0)
MI1	- Unita' dei minuti	- 4 bit meno significativi MI1(3-0)
MI10	- Decine dei minuti	- 3 bit meno significativi MI10(2-0)
H1	- Unita' delle ore	- 4 bit meno significativi H1(3-0)
H10	- Decine delle ore	- 2 bit meno significativi H10(1-0)
	Il terzo bit di tale registro H10(2) indica l' AM/PM	
G1	- Unita' del giorno	- 4 bit meno significativi D1(3-0)
G10	- Decine del giorno	- 2 bit meno significativi D10(1-0)
ME1	- Unita' del mese	- 4 bit meno significativi MO1(3-0)
ME10	- Decine del mese	- 1 bit meno significativo MO10(0)
A1	- Unita' dell' anno	- 4 bit meno significativi Y1(3-0)
A10	- Decine dell' anno	- 4 bit meno significativi Y10(3-0)
GS	- Giorno della settimana	- 3 bit meno significativi W(2-0)

Per quest' ultimo registro vale la corrispondenza:

GS2	GS1	GS0	
0	0	0	Domenica
0	0	1	Lunedi'
0	1	0	Martedi'
0	1	1	Mercoledi'
1	0	0	Giovedi'
1	0	1	Venerdi'
1	1	0	Sabato

I tre registri di controllo sono invece utilizzati come segue:

bit 7 6 5 4 3 2 1 0
REG D = NU NU NU NU 30S IF B H
dove:
NU = Non usato
30S = Se attivo (1) permette di effettuare una correzione di 30 secondi dell' orario.
IF = Indica se il contatore interno è attivato o se si è verificata una interruzione: 1 -> interruzione e viceversa.
B = Indica se possono essere effettuate operazioni di R/W dei registri: 1 -> operazioni impossibili.
H = Se attivo (1) effettua la memorizzazione dell' orario fissato.

bit 7 6 5 4 3 2 1 0
REG E = NU NU NU NU T1 T0 I M
dove:
NU = Non usato.
T1 T0 = Determinano la durata del ciclo di interruzione dei contatori interni.
0 0 -> 1/64 secondo
0 1 -> 1 secondo
1 0 -> 1 minuto
1 1 -> 1 ora
I = Se attivo (1) abilita la durata del ciclo di interruzione pari a quella selezionata con T1 e T0, altrimenti tale durata è normalizzata internamente.
M = Se attivo (1) disabilita il pin 1 /STD del RTC, ovvero il pin che riporta il segnale interno di conteggio.

bit 7 6 5 4 3 2 1 0
REG F = NU NU NU NU T 24/12 S R
dove:
NU = Non usato.
T = Stabilisce da quale contatore interno prelevare il segnale di conteggio:
1 -> contatore principale; 0 -> 15' contatore.
24/12 = Stabilisce il modo di conteggio delle ore:
1 -> 1-24; 0 -> 1-12 con AM/PM.
S = Se attivo (1) provoca l' arresto dell' avanzamento dell' orologio fino alla sucessiva abilitazione.
R = Se attivo (1) provoca il reset di tutti i contatori interni.

Il 72421 gestisce anche un uscita (/STD pin 1) attraverso cui puo' emettere dei segnali periodici con periodo programmabile ,per poter generare nei confronti della CPU ,dei segnali di /INT.
L'abilitazione di dette linee viene gestita dal jumper J1.

DIREZIONALITÀ DELLA COMUNICAZIONE IN RS 422-485

Per gestire la direzione nella comunicazione in RS 485 o l'attivazione del driver di trasmissione nella comunicazione RS 422, sulla **GPC® 114** viene utilizzata un'apposita linea digitale di I/O del microprocessore, denominata DIR. Tale linea è collegata direttamente al pin 22 della CPU (PD.2) e come descritto nel paragrafo "SELEZIONE DEL TIPO DI COMUNICAZIONE SERIALE" ha la seguente funzione:

- RS 485:	DIR = 0	->	Linea seriale RS 485 in ricezione
	DIR = 1	->	Linea seriale RS 485 in trasmissione
- RS 422:	DIR = 0	->	Trasmettitore RS 422 disattivo
	DIR = 1	->	Trasmettitore RS 422 attivo

In fase di reset o power on, il segnale DIR è mantenuto a livello logico basso di conseguenza in seguito ad una di queste fasi il driver 485 è in ricezione o il driver di trasmissione 422 è disattivo, in modo da eliminare eventuali conflittualità sulla linea di comunicazione.

SCHEDE ESTERNE

La scheda **GPC® 114** si interfaccia a buona parte dei moduli della serie BLOCK e di interfaccia utente. Le risorse di bordo possono essere facilmente aumentate collegando la **GPC® 114** alle numerose schede periferiche del carteggio **grifo®** tramite l'**ABACO®** I/O BUS. Anche schede in formato Europa con BUS **ABACO®** possono essere collegate, sfruttando gli appositi mother boards. A titolo di esempio ne riportiamo un elenco con una breve descrizione delle carratteristiche di massima, per maggiori informazioni, richiedere la documentazione specifica:

OBI 01 - OBI 02

Opto BLOCK Input NPN-PNP

Interfaccia per 16 input optoisolati e visualizzati tipo NPN, PNP, connettore a morsettiera, connettore normalizzato I/O **ABACO®** a 20 vie; sezione alimentatrice; attacco rapido per guide DIN 46277-1 e 3.

OBI N8 - OBI P8

Opto BLOCK Input NPN-PNP

Interfaccia per 8 input optoisolati e visualizzati tipo NPN, PNP, connettore a morsettiera, connettore normalizzato I/O **ABACO®** a 20 vie; sezione alimentatrice; attacco rapido per guide DIN 46277-1 e 3.

TBO 01 - TBO 08

Transistor BLOCK Output

Interfaccia per 16 connettore normalizzato I/O **ABACO®** a 20 vie; 16 o 8 output a transistor in Open Collector da 45 Vdc 3 A su connettore a morsettiera. Uscite optoisolate e visualizzate; attacco rapido per guide DIN 6277-1 e 3.

RBO 01

Relè BLOCK Output

Interfaccia per connettore normalizzato I/O **ABACO®** a 20 vie; 8 output visualizzati con relè da 5 o 10 A (connettore a morsettiera); contatti in scambio (N.O. e N.C.); attacco rapido per guide DIN 46277-1 e 3.

RBO 08 - RBO 16

Relè BLOCK Output

Interfaccia per connettore normalizzato I/O **ABACO®** a 20 vie; 8 o 16 output visualizzati con relè da 3 A con MOV; connettore a morsettiera; attacco rapido per guide DIN 46277-1 e 3.

XBI 01

miXed BLOCK Input-Output

Interfaccia tra 8 input + 8 output TTL (connettore normalizzato I/O **ABACO®** a 20 vie), con 8 output a transistor in Open Collector da 45 Vdc 3 A + 8 input con filtro a Pi-Greco (connettore a morsettiera). I/O optoisolati e visualizzati; attacco rapido per guide DIN 46277-1 e 3.

XBI R4 - XBI T4

miXed BLOCK Input-Output

Interfaccia per connettore normalizzato I/O **ABACO®** a 20 vie; 4 relè da 3 A con MOV o 4 transistor open collectors da 3 A optoisolati; 4 linee di input optoisolate; linee di I/O visualizzate; connettore a morsettiera; attacco rapido per guide DIN tipo C e guide Ω.

FBC 20 - FBC 120

Flat Block Contact 20 vie

Interfaccia tra 2 o 1 connettori a perforazione di isolante (scatolino da 20 vie maschi) e la filatura da campo (morsettiere a rapida estrazione). Attacco rapido per guide tipo DIN 46277-1 e 3.

IBC 01

Interface Block Comunication

Scheda di conversioni per comunicazioni seriali. 2 linee RS 232; 1 linea RS 422-485; 1 linea in fibra ottica; interfaccia DTE/DCE selezionabile; attacco rapido per guide tipo DIN 46277-1 e 3.

IAC 01

Interface Adapter Centronics

Interfaccia tra 16 I/O TTL su connettore normalizzato I/O **ABACO®** a 20 vie e connettore a vaschetta D 25 vie femmina con pin out standard Centronics per la gestione di una stampante parallela.

DEB 01

Didactis Experimental Board

Scheda di supportro per l'utilizzo di 16 linee di I/O TTL. Comprende: 16 tasti; 16 LED; 4 digits; tastiera a matrice da 16 tasti; interfaccia per stampante Centronics, dislay LCD, display Fluorescente, connettore I/O **GPC® 68**; collegamento con il campo.

MCI 64

Memory Cards Interfaces 64 MBytes

Interfaccia per la gestione di Memory cards PCMCIA a 68 pins tramite un connettore normalizzato I/O **ABACO®**; sono disponibili driver per linguaggi ad alto livello.

KDL X24 - KDF 224

Keyboard Display LCD 2,4 righe 24 tasti - Keyboard Display Fluorescent 2 righe 24 tasti

Interfaccia tra 16 I/O TTL su connettore normalizzato I/O **ABACO®** a 20 vie e tastiera a matrice esterna da 24 tasti; display alfanumerico fluorescente 20x 2 o LCD 20x2, 20x4 retroilluminato a LEDs. Predisposizione per collegamento a tastiera telefonica.

QTP 24P

Quick Terminal Panel 24 tasti con interfaccia Parallela

Interfaccia operatore provvista di display alfanumerico fluorescente 20x 2 o LCD 20x2, 20x4 retroilluminato a LEDs; tastiera a membrana da 24 tasti di cui 12 configurabili dall'utente; 16 LEDs di stato; alimentatore a bordo scheda in grado di pilotare anche carichi esterni; interdaccia parallela basata su 16 I/O TTL di un connettore normalizzato I/O **ABACO®** a 20 vie. Tasti ed etichette personalizzabili tramite serigrafie da inserire in apposite tasche; opzione di contenitore metallico.

QTP G26

Quick Terminal Panel 26 tasti con LCD grafico

Interfaccia operatore provvista di display grafico da 240x128 pixel retroilluminato a LEDs; tastiera a membrana da 26 tasti di cui 6 configurabili dall'utente; 16 LEDs di stato; alimentatore a bordo scheda; interdaccia seriale in RS 232, RS 422-485 o current loop; linea seriale ausiliaria in RS 232 Tasti ed etichette personalizzabili dall'utente tramite serigrafie da inserire in apposite tasche; contenitore metallico e plastico; EEPROM di set up; 256K EPROM o FLASH; Real Time Clock; 128K RAM; buzzer. Firmware di gestione che svolge funzione di terminale con primitive grafiche.

ZBR xxx

Zipped BLOCK Relays xx Input + xx Output

Periferica per xx Input optoisolati e visualizzati tipo NPN; xx relè da 3A con MOV; connettori a morsettiera per ingressi optoisolati e uscite; connettore normalizzato **ABACO®** I/O BUS; 61 LEDs di visualizzazione; sezione alimentatrice a bordo; attacco rapide per guide Ω. Le possibili configurazioni in termini di numero di I/O sono: xxx=324 con 32 In e 24 Out; xxx=246 con 24 In e 16 Out; xxx=168 con 16 In e 8 Out.

ZBT xxx

Zipped BLOCK Transistors xx Input + xx Output

Periferica per xy Input optoisolati e visualizzati tipo NPN; yz darlinghton da 3A con diodo di ricircolo; connettori a morsettiera per ingressi optoisolati e uscite; connettore normalizzato **ABACO®** I/O BUS; 61 LEDs di visualizzazione; sezione alimentatrice a bordo; attacco rapide per guide Ω. Le possibili configurazioni in termini di numero di I/O sono: xxx=324 con 32 In e 24 Out; xxx=246 con 24 In e 16 Out; xxx=168 con 16 In e 8 Out.

ABB 05

Abaco® Block BUS 5 slots

Mother board **ABACO®** da 5 slots; passo 4 TE; guidaschede; connettori normalizzati di alimentazione; tasto di reset; LEDs per alimentazioni; interfaccia **ABACO®** I/O BUS; sezione alimentatrice per +5 Vdc; sezione alimentatrice per +V Opto; sezioni alimentatrici galvanicamente isolate; tre tipi di alimentazione: da rete, bassa tensione o stabilizzata. Attacco rapido per guide Ω.

ABB 03

Abaco® Block BUS 3 slots

Mother board **ABACO®** da 3 slots; passo 4 TE; guidaschede; connettori normalizzati di alimentazione; tasto di reset; LEDs per alimentazioni; interfaccia **ABACO®** I/O BUS. Attacco rapido per guide Ω.

BIBLIOGRAFIA

È riportato di seguito, un elenco di manuali e note tecniche, a cui l'utente può fare riferimento per avere maggiori chiarimenti, sui vari componenti montati a bordo della scheda **GPC® 114**.

Manuale MAXIM:	*New Releases Data Book - Volume 4*
Manuale MOTOROLA:	*M68HC11 HCMOS Single-chip Microcomputer*
Manuale NEC:	*Memory Products*
Manuale TEXAS INSTRUMENTS:	*The TTL Data Book - SN54/74 Families*
Manuale TEXAS INSTRUMENTS:	*Linear Circuits Dtata Book - Volumi 1 e 3*
Manuale TEXAS INSTRUMENTS:	*RS-422 and RS-485 Interface Circuits*
Documentazione SEIKO EPSON:	*REAL TIME CLOCK MODULE RTC-72421 Application manual*

Per avere tutti gli aggiornamenti di tali manuali e di tutti i data-sheet fare riferimento ai siti in INTERNET delle case madri costruttrici.

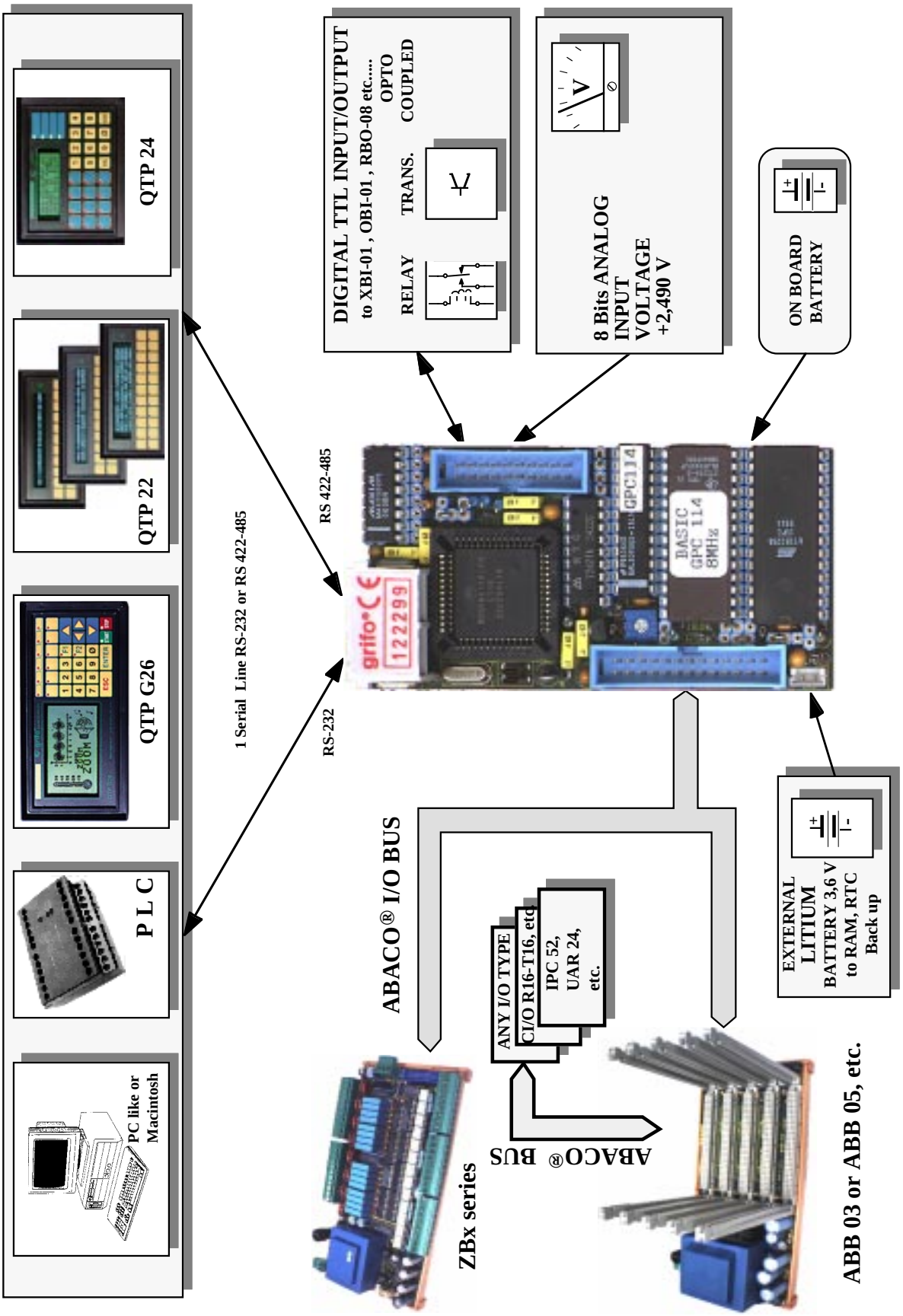


FIGURA 27: SCHEMA DELLE POSSIBILI CONNESSIONI PER GPC®114

APPENDICE A: DISPOSIZIONE JUMPERS E DRIVERS SERIALI

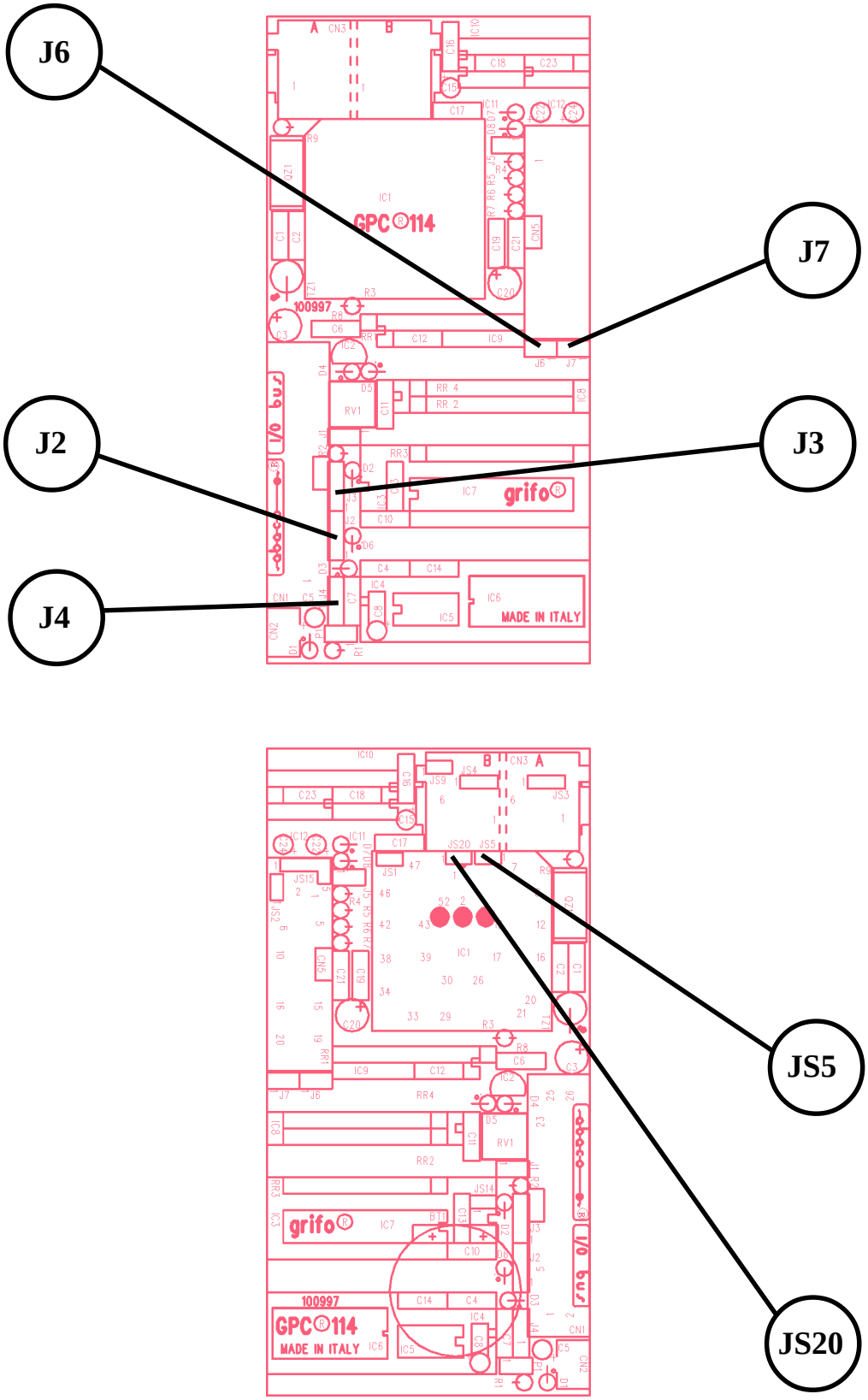


FIGURA 28: DISPOSIZIONE JUMPERS PER MEMORIE

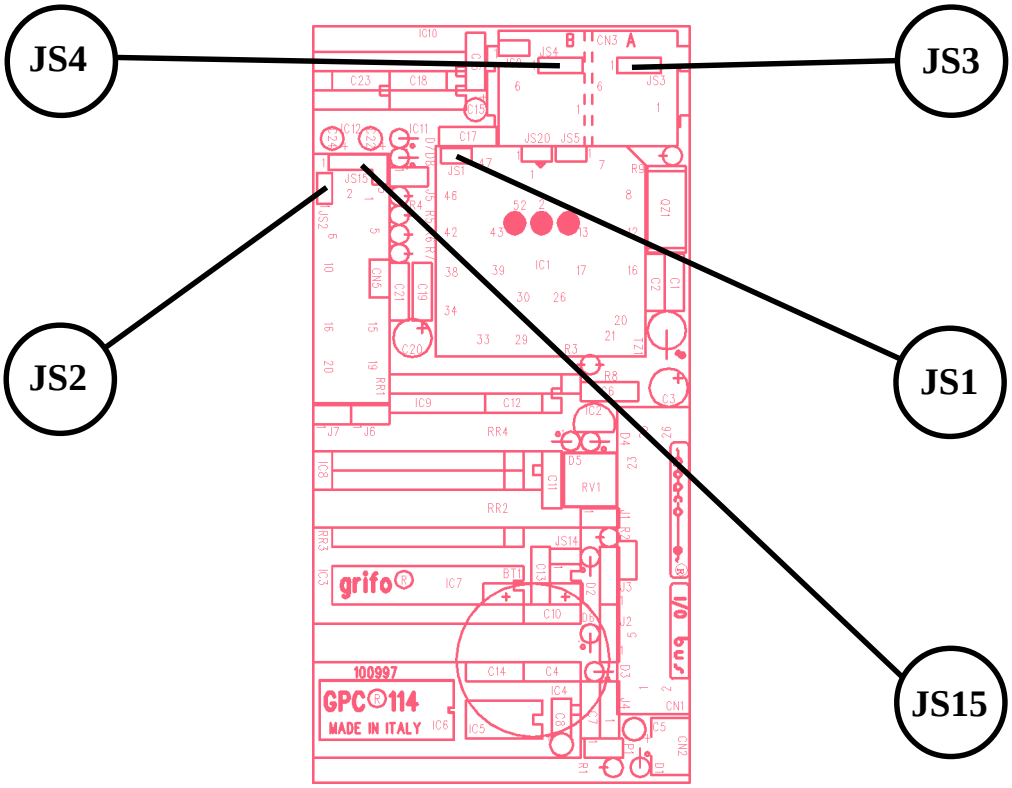
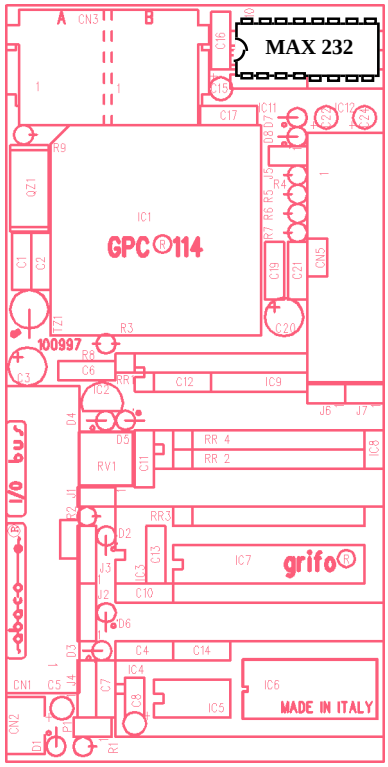
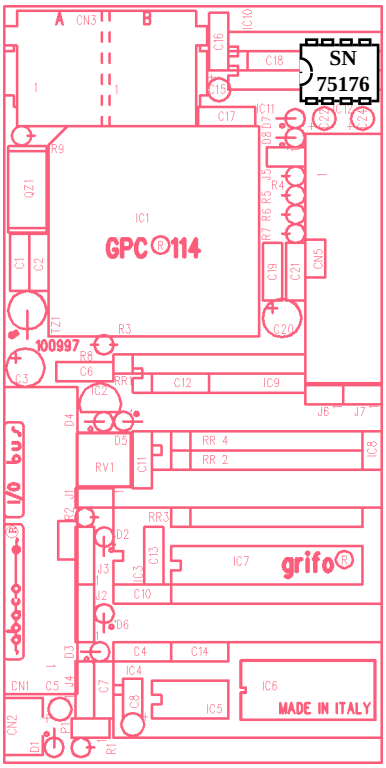


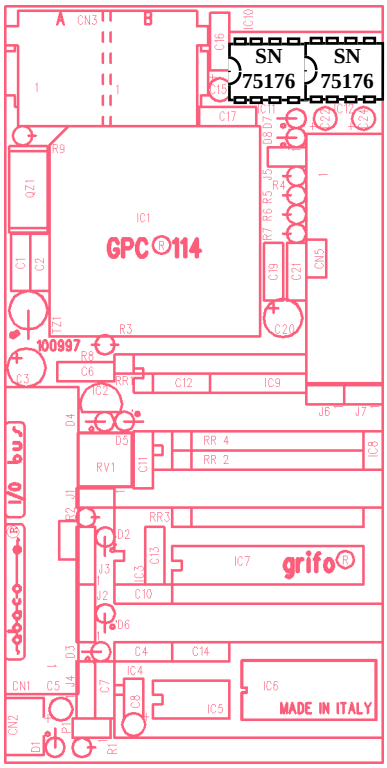
FIGURA 29: DISPOSIZIONE JUMPERS PER COMUNICAZIONE SERIALE



RS 232



RS 485



RS 422

FIGURA 30: DISPOSIZIONE DRIVERS PER COMUNICAZIONE SERIALE

APPENDICE B: DESCRIZIONE COMPONENTI DI BORDO

Di seguito vengono riportate le pagine salienti del micro controllore 68HC11A8 che si differenzia dalla versione A1, solamente dal fatto che A1 non ha 8K di ROM disponibile per l'utente, ma possiede il ROM BUFFALO.

B MECHANICAL DATA AND ORDERING INFORMATION

B.1 Pin Assignments

The MC68HC11A8 is available in the 52-pin plastic leaded chip carrier (PLCC), the 48-pin dual in-line package (DIP), or the 64-pin quad flat pack (QFP).

A8 52-PIN PLCC

Figure B-1 52-Pin PLCC

1 INTRODUCTION

The HCMOS MC68HC11A8 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. A fully static design and high-density complementary metal-oxide semiconductor (HCMOS) fabrication process allow E-series devices to operate at frequencies from 3 MHz to dc, with very low power consumption.

1.1 Features

The following are some of the hardware and software highlights.

1.1.1 Hardware Features

- 8 Kbytes of ROM
- 512 Bytes of EEPROM
- 256 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  - Four Stage Programmable Prescaler
  - Three Input Capture Functions
  - Five Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Dual-In-Line or Leaded Chip Carrier Packages

1.1.2 Software Features

- Enhanced M6800/M6801 Instruction Set
- 16 x 16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

1.2 General Description

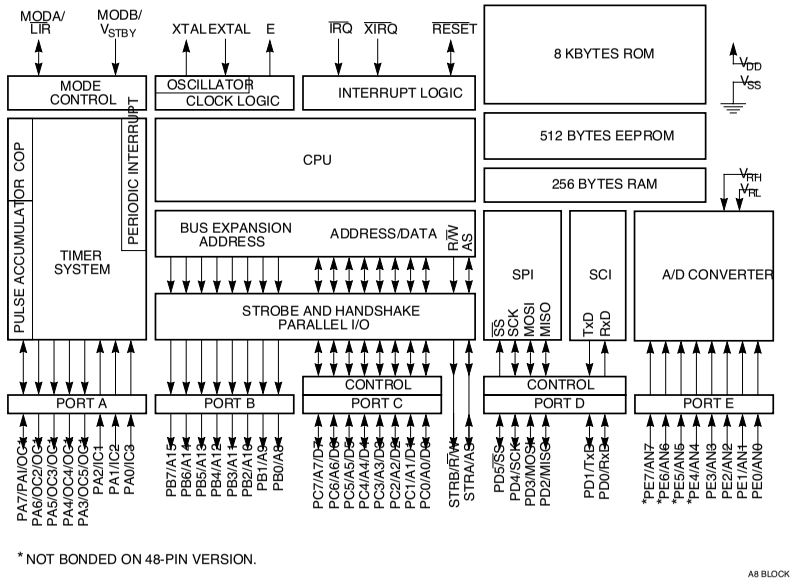
The high-density CMOS technology (HCMOS) used on the MC68HC11A8 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 8 Kbytes of ROM, 512 bytes of electrically erasable programmable ROM (EEPROM), and 256 bytes of static RAM.

A block diagram of the MC68HC11A8 is shown in **Figure 1-1**. Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface

(SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.



* NOT BONDED ON 48-PIN VERSION.

Figure 1-1 Block Diagram

1.3 Programmer's Model

In addition to being able to execute all M6800 and M6801 instructions, the MC68HC11A8 allows execution of 91 new opcodes. **Figure 1-2** shows the seven CPU registers which are available to the programmer.

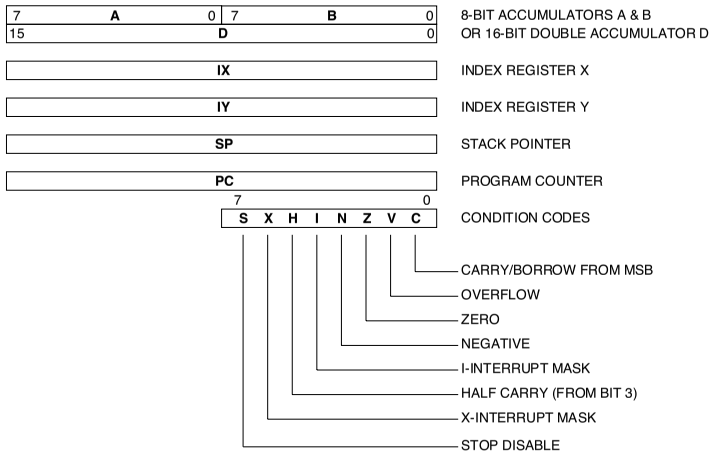


Figure 1-2 Programming Model

1.4 Summary of M68HC11 Family

Table 1-1 and the following paragraphs summarize the current members of the M68HC11 family of MCUs. This technical data book describes the MC68HC11A8 version and can be used as a primary reference for several other versions of the M68HC11 family. However, with the exception of the CPU, some newer members differ greatly from the MC68HC11A8 MCU and their respective technical literature should be referenced.

Several of the device series within the M68HC11 family have ′x1 and ′x0 versions. These are identical to the main member of the series but have some of their on-chip resources disabled. For instance, an MC68HC11A1 is identical to the MC68HC11A8 except that its ROM is disabled. An MC68HC11A0 has disabled EPROM **and** EEPROM arrays. Refer to **Table 1-1**.

Nearly all series within the M68HC11 family have both a ROM version and an EPROM version. Any device in the M68HC11 family that has a 7 preceding the 11 is a device containing EPROM instead of ROM (e.g., MC68HC711E9). These devices operate exactly as the custom ROM-based version (e.g., MC68HC11E9) but can be programmed by the user. EPROM-based devices in a windowed package can be erased and reprogrammed indefinitely. EPROM-based devices in standard packages are one-time-programmable (OTP). Refer to **Table 1-1**.

Table 1-1 M68HC11 Family Devices

Device	RAM	ROM	EPROM	EEPROM	COMMENTS
MC68HC11A8	256	8K	0	512	16-bit timer; 8 channel 8-bit A/D, SCI, SPI
MC68HC11A7	256	8K	0	0	
MC68HC11A1	256	0	0	512	
MC68HC11A0	256	0	0	0	
MC68HC11D3	192	4K	0	0	16-bit timer; SCI, SPI
MC68HC711D3	192	0	4K	0	
MC68HC11D0	192	0	0	0	
MC68HC11ED0	512	0	0	0	16-bit timer; SCI, SPI
MC68HC11E9	512	12K	0	512	16-bit timer; SCI, SPI, 8 channel 8-bit A/D
MC68HC711E9	512	0	12K	512	
MC68HC11E8	512	12K	0	0	
MC68HC11E1	512	0	0	512	
MC68HC11E0	512	0	0	0	
MC68HC811E2	256	0	0	2048	16-bit timer; SCI, SPI, 8 channel 8-bit A/D, 2K EEPROM
MC68HC11E20	768	20K	0	512	16-bit timer; SCI, SPI, 8 channel 8-bit A/D,
MC68HC711E20	768	0	20K	512	20K ROM/EPROM
MC68HC11F1	1024	0	0	512	nonmultiplexed bus, 8 channel 8-bit A/D, 4 chip selects, SCI, SPI
MC68HC11G7	512	24K	0	0	nonmultiplexed bus, 8 channel 10-bit A/D, 4 channel PWM,
MC68HC11G5	512	16K	0	0	SCI, SPI, 66 I/O pins
MC68HC711G5	512	0	16K	0	
MC68HC11G0	512	0	0	0	
MC68HC11K4	768	24K	0	640	nonmultiplexed bus, memory expansion to 1MB,
MC68HC711K4	768	0	24K	640	8 channel 8-bit A/D, 4 channel PWM, 4 chip selects
MC68HC11K3	768	24K	0	0	
MC68HC11K1	768	0	0	640	
MC68HC11K0	768	0	0	0	
MC68HC11KA4	768	24K	0	640	nonmultiplexed bus, 8 channel 8-bit A/D, SCI, SPI,
MC68HC711KA4	768	0	24K	640	4 channel PWM
MC68HC11KA2	1024	32K	0	640	
MC68HC711KA2	1024	0	32K	640	
MC68HC11L6	512	16K	0	512	multiplexed bus, 16-bit timer; 8 channel 8-bit A/D, SCI, SPI
MC68HC711L6	512	0	16K	512	
MC68HC11L5	512	16K	0	0	
MC68HC11L1	512	0	0	512	
MC68HC11L0	512	0	0	0	
MC68HC11M2	1280	32K	0	640	nonmultiplexed bus, 8 channel 8-bit A/D, 4 channel PWM,
MC68HC711M2	1280	0	32K	640	DMA, on-chip math coprocessor, SCI, 2 SPI
MC68HC11N4	768	24K	0	640	nonmultiplexed bus, 12 channel 8-bit A/D, 2 channel 8-bit D/A,
MC68HC711N4	768	0	24K	640	6 channel PWM, on-chip math coprocessor, SCI, SPI
MC68HC11P2	1024	32K	0	640	nonmultiplexed bus, PLL, 8 channel 8-bit A/D, 4 channel PWM,
MC68HC711P2	1024	0	32K	640	3 SCI (2 with MI bus), SPI, 62 I/O pins

2.1.4 E Clock Output (E)

This is the output connection for the internally generated E clock which can be used as a timing reference. The frequency of the E clock output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. When the E clock output is low an internal process is taking place and, when high, data is being accessed. The E clock signal is halted when the MCU is in STOP mode.

2.1.5 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means for requesting asynchronous interrupts to the MC68HC11A8. It is program selectable (OPTION register) with a choice of either negative edge-sensitive or level-sensitive triggering, and is always configured to level-sensitive triggering by reset. The $\overline{IRQ}$ pin requires an external pull-up resistor to V_{DD} (typically 4.7K ohm).

2.1.6 Non-Maskable Interrupt ($\overline{XIRQ}$)

This input provides a means for requesting a non-maskable interrupt, after reset initialization. During reset, the X bit in the condition code register is set and any interrupt is masked until MCU software enables it. The $\overline{XIRQ}$ input is level sensitive and requires an external pull-up resistor to V_{DD}.

2.1.7 Mode A/Load Instruction Register and Mode B/Standby Voltage (MODA/$\overline{LIR}$, MODB/V_{STBY})

During reset, MODA and MODB are used to select one of the four operating modes. Refer to **Table 2-1**. Paragraph **2.2 Operating Modes** provides additional information.

Table 2-1 Operating Modes vs. MODA and MODB

MODB	MODA	Mode Selected
1	0	Single Chip
1	1	Expanded Multiplexed
0	0	Special Bootstrap
0	1	Special Test

After the operating mode has been selected, the $\overline{LIR}$ pin provides an open-drain output to indicate that an instruction is starting. All instructions are made up of a series of E clock cycles. The $\overline{LIR}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided as an aid in program debugging.

The V_{STBY} signal is used as the input for RAM standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal 256-byte RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

3 ON-CHIP MEMORY

This section describes the on-chip ROM, RAM, and EEPROM memories. The memory maps for each mode of operation are shown and the RAM and I/O mapping register (INIT) is described. The INIT register allows the on-chip RAM and the 64 control registers to be moved to suit the needs of a particular application.

3.1 Memory Maps

Composite memory maps for each mode of operation are shown in **Figure 3-1**. Memory locations are shown in the shaded areas and the contents of these shaded areas are shown to the right. These modes include single-chip, expanded multiplexed, special bootstrap, and special test.

Single-chip operating modes do not generate external addresses. Refer to **Table 3-1** for a full list of the registers.

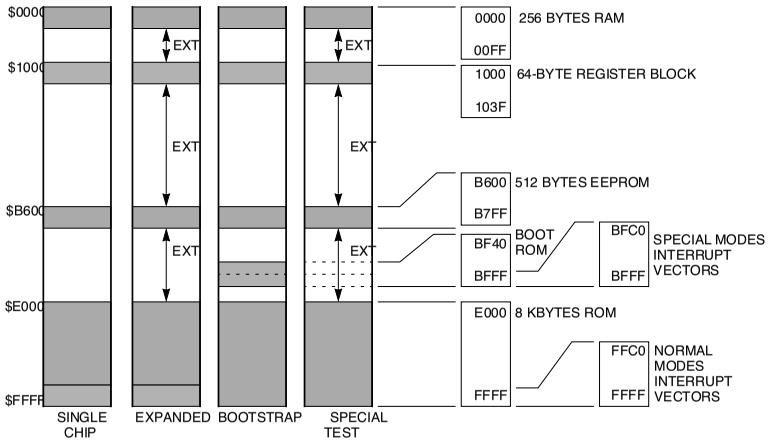


Figure 3-1 Memory Maps

Table 3-1 Register and Control Bit Assignments (Sheet 1 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	–	–	–	–	–	–	Bit 0	PORTA	I/O Port A
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control R
$1003	Bit 7	–	–	–	–	–	–	Bit 0	PORTC	I/O Port C
$1004	Bit 7	–	–	–	–	–	–	Bit 0	PORTB	Output Port B
$1005	Bit 7	–	–	–	–	–	–	Bit 0	PORTCL	Alternate Latched Port C
$1006									Reserved	
$1007	Bit 7	–	–	–	–	–	–	Bit 0	DDRC	Data Direction for Port C
$1008			Bit 5	–	–	–	–	Bit 0	PORTD	I/O Port D
$1009			Bit 5	–	–	–	–	Bit 0	DDRD	Data Direction for Port D
$100A	Bit 7	–	–	–	–	–	–	Bit 0	PORTE	Input Port E
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Regist
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Reg
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Reg
$100E	Bit 15	–	–	–	–	–	–	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	–	–	–	–	–	–	Bit 0		
$1010	Bit 15	–	–	–	–	–	–	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	–	–	–	–	–	–	Bit 0		
$1012	Bit 15	–	–	–	–	–	–	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	–	–	–	–	–	–	Bit 0		
$1014	Bit 15	–	–	–	–	–	–	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	–	–	–	–	–	–	Bit 0		
$1016	Bit 15	–	–	–	–	–	–	Bit 8	TOC1	Output Compare 1 Register
$1017	Bit 7	–	–	–	–	–	–	Bit 0		
$1018	Bit 15	–	–	–	–	–	–	Bit 8	TOC2	Output Compare 2 Register
$1019	Bit 7	–	–	–	–	–	–	Bit 0		
$101A	Bit 15	–	–	–	–	–	–	Bit 8	TOC3	Output Compare 3 Regi
$101B	Bit 7	–	–	–	–	–	–	Bit 0		
$101C	Bit 15	–	–	–	–	–	–	Bit 8	TOC4	Output Compare 4 Register
$101D	Bit 7	–	–	–	–	–	–	Bit 0		
$101E	Bit 15	–	–	–	–	–	–	Bit 8	TCO5	Output Compare 5 Regi
$101F	Bit 7	–	–	–	–	–	–	Bit 0		

Table 3-1 Register and Control Bit Assignments (Sheet 2 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
$1021			EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Reg
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Reg
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Regist
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Register
$1026	DDRA7	PAEN	PAMOD	PEDGE			RTR1	RTR0	PACTL	Pulse Accumulator Contr
$1027	Bit 7	—	—	—	—	—	—	Bit 0	PACNT	Pulse Accumulator Count Re
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
$102A	Bit 7	—	—	—	—	—	—	Bit 0	SPDR	SPI Data Register
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register 2
$102E	TRDE	TC	RDRF	IDLE	OR	NF	FE		SCSR	SCI Status Register
$102F	Bit 7	—	—	—	—	—	—	Bit 0	SCDR	SCI Data (Read RDR, Write TDR
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	—	—	—	—	—	—	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	—	—	—	—	—	—	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	—	—	—	—	—	—	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	—	—	—	—	—	—	Bit 0	ADR4	A/D Result Register 4
$1035 thru $1038									Reserved	
$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Opt
$103A	Bit 7	—	—	—	—	—	—	Bit 0	COPRST	Arm/Reset COP Timer Circu
$103B	ODD	EVEN		BYTE	ROW	ERASE	EELAT	EEPGM	PPROG	EEPROM Program Control Register
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Priority I-Bit Int
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping R
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Re
$103F	—	—	—	—	NOSEC	NOCOP	ROMON	EEON	CONFIG	COP, ROM, and EEPROI

In expanded multiplexed operating modes, memory locations are basically the same as the single- chip operating modes; however, the locations between the shaded areas (designated EXT) are for externally addressed memory and I/O. If an external memory or I/O device is located to overlap an enabled internal resource, the internal resource will take priority. For reads of such an address the data (if any) driving the port C data inputs is ignored and will not result in any harmful conflict with the internal read. For writes to such an address data is driven out of the port C data pins as well as to the internal location. No external devices should drive port C during write accesses to internal locations; however, there is normally no conflict since the external address decode and/ or data direction control should incorporate the R/$\overline{W}$ signal in their development. The R/$\overline{W}$, AS, address, and write data signals are valid for all accesses including accesses to internal memory and registers.

The special bootstrap operating mode memory locations are similar to the single-chip operating mode memory locations except that a bootstrap program at memory locations $BF40 through $BFFF is enabled. The reset and interrupt vectors are addressed at $BFC0–$BFFF while in the special bootstrap operating mode. These vector addresses are within the 192 byte memory used for the bootstrap program.

The special test operating mode memory map is the same as the expanded multiplexed operating mode memory map except that the reset and interrupt vectors are located at external memory locations $BFC0–$BFFF.

3.2 RAM and I/O Mapping Register (INIT)

There are 64 internal registers which are used to control the operation of the MCU. These registers can be relocated on 4K boundaries within the memory space, using the INIT register. Refer to **Table 3-1** for a complete list of the registers. The registers and control bits are explained throughout this document.

The INIT register is a special-purpose 8-bit register which may be used during initialization to change the default locations of RAM and control registers within the MCU memory map. It may be written to only once within the initial 64 E clock cycles after a reset and thereafter becomes a read-only register.

	7	6	5	4	3	2	1	0	
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
RESET	0	0	0	0	0	0	0	1	

The default starting address for internal RAM is $0000 and the default starting address for the 64 control registers is $1000 (the INIT register is set to $01 at reset). The upper four bits of the INIT register specify the starting address for the 256 byte RAM and the lower four bits of INIT specify the starting address for the 64 control registers. These four bits are matched to the upper four bits of the 16-bit address.

Throughout this document, the control register addresses will be displayed with the high-order digit shown as a bold "**1**" to indicate that the register block may be relocated to some 4K memory page other than its default position of $1000-$103F.

Note that if the RAM is relocated to either $E000 or $F000, which is in conflict with the internal ROM, (no conflict if the ROMON bit in the configuration register is zero), RAM will take priority and the conflicting ROM will become inaccessible. Also, if the 64 control registers are relocated so that they conflict with the RAM and/or ROM, then the 64 control registers take priority and the RAM and/or ROM at those locations become inaccessible. No harmful conflicts result, the lower priority resources simply become inaccessible. Similarly, if an internal resource conflicts with an external device no harmful conflict results. Data from the external device will not be applied to the internal data bus and cannot interfere with the internal read.

Note that there are unused register locations in the 64 byte control register block. Reads of these unused registers will return data from the undriven internal data bus and not from another resource that happens to be located at the same address.

3.3 ROM

The internal 8K ROM occupies the highest 8K of the memory map ($E000–$FFFF). This ROM is disabled when the ROMON bit in the CONFIG register is clear. The ROMON bit is implemented with an EEPROM cell and is programmed using the same procedures for programming the on-chip EEPROM. For further information refer to **3.5.3 System Configuration Register (CONFIG)**.

In the single-chip operating mode, internal ROM is enabled regardless of the state of the ROMON bit.

There is also a 192 byte mask programmed boot ROM in the MC68HC11A8. This bootstrap program ROM controls the operation of the special bootstrap operating mode and is only enabled following reset in the special bootstrap operating mode. For more information refer to **2.2.3 Special Bootstrap Operating Mode.**

3.4 RAM

The 256 byte internal RAM may be relocated during initialization by writing to the INIT register. The reset default position is $0000 through $00FF. This RAM is implemented with static cells and retains its contents during the WAIT and STOP modes.

The contents of the 256-byte RAM can also be retained by supplying a low current backup power source to the MODB/V_{STBY} pin. When using a standby power source, V_{DD} may be removed; however, $\overline{\text{RESET}}$ must go low before V_{DD} is removed and remain low until V_{DD} has been restored.

3.5 EEPROM

The 512 bytes of EEPROM are located at $B600 through $B7FF and have the same read cycle time as the internal ROM. The write (or programming) mechanism for the EEPROM is controlled by the PPROG register. The EEPROM is disabled when the EEON bit in the CONFIG register is zero. The EEON bit is implemented with an EEPROM cell.

The erased state of an EEPROM byte is $FF. Programming changes ones to zeros. If any bit in a location needs to be changed from a zero to a one, the byte must be erased in a separate operation before it is reprogrammed. If a new data byte has no ones in bit positions which were already programmed to zero, it is acceptable to program the new data without erasing the EEPROM byte first. For example, programming $50 to a location which was already $55 would change the location to $50.

Programming and erasure of the EEPROM relies on an internal high-voltage charge pump. At E clock frequencies below 2 MHz the efficiency of this charge pump decreases which increases the time required to program or erase a location. The recommended program and erase time is 10 milliseconds when the E clock is 2 MHz and should be increased to as much as 20 milliseconds when E is between 1 MHz and 2 MHz. When the E clock is below 1 MHz, the clock source for the charge pump should be switched from the system clock to an on-chip R-C oscillator clock. This is done by setting the CSEL bit in the OPTION register. A 10 millisecond period should be allowed after setting the CSEL bit to allow the charge pump to stabilize. Note that the CSEL bit also controls a clock to the analog-to-digital converter subsystem.

3.5.1 EEPROM Programming Control Register (PPROG)

This 8-bit register is used to control programming and erasure of the 512-byte EEPROM. Reset clears this register so the EEPROM is configured for normal reads.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
RESET	0	0	0	0	0	0	0	0	

ODD — Program Odd Rows (TEST)

EVEN — Program Even Rows (TEST)

Bit 5 — Not implemented.
This bit always reads zero.

BYTE — Byte Erase Select
This bit overrides the ROW bit.
0 = Row or Bulk Erase
1 = Erase Only One Byte

ROW — Row Erase Select
If the BYTE bit is 1, ROW has no meaning.
0 = Bulk Erase
1 = Row Erase

ERASE — Erase Mode Select
0 = Normal Read or Program
1 = Erase Mode

EELAT — EEPROM Latch Control
0 = EEPROM Address and Data Configured for Read Mode
1 = EEPROM Address and Data Configured for Programming/Erasing

EEPGM — EEPROM Programming Voltage Enable
0 = Programming Voltage Switched Off
1 = Programming Voltage Turned On

If an attempt is made to set both the EELAT and EEPGM bits in the same write cycle, neither will be set. If a write to an EEPROM address is performed while the EEPGM bit is set, the write is ignored and the programming operation currently in progress is not disturbed. These two safeguards were included to prevent accidental EEPROM changes in cases of program runaway. Mask sets A38P, A49N, and date codes before 86xx did not have these safeguards.

3.5.2 Programming/Erasing Internal EEPROM

The EEPROM programming and erasure process is controlled by the PPROG register. The following paragraphs describe the various operations performed on the EEPROM and include example program segments to demonstrate programming and erase operations.

These program segments are intended to be simple straightforward examples of the sequences needed for basic program and erase operations. There are no special restrictions on the address modes used and bit manipulation instructions may be used. Other MCU operations can continue to be performed during EEPROM programming and erasure provided these operations do not include reads of data from EEPROM (the EEPROM is disconnected from the read data bus during EEPROM program and erase operations). The subroutine DLY10 used in these program segments is not shown but can be any set of instructions which takes ten milliseconds.

3.5.2.1 Read

For the read operation the EELAT bit in the PPROG register must be clear. When this bit is cleared, the remaining bits in the PPROG register have no meaning or effect, and the EEPROM may be read as if it were a normal ROM.

3.5.2.2 Programming

During EEPROM programming, the ROW and BYTE bits are not used. If the E clock frequency is 1 MHz or less, the CSEL bit in the OPTION register must be set. Recall that in this EEPROM, zeros must be erased by a separate erase operation before programming. The following program segment demonstrates how to program an EEPROM byte.


```
* On entry, A = data to be programmed and X = EEPROM address
        •
        •
        •
PROG    LDAB    #$02
        STAB    $103B   Set EELAT Bit (EEPGM = 0)
        STAA    0,X     Store Data to EEPROM Address
        LDAB    #$03
        STAB    $103B   Set EEPGM Bit (EELAT = 1)
        JSR     DLY10   Delay 10 ms
        CLR     $103B   Turn Off High Voltage and Set to READ
                        Mode
        •
        •
        •
```

3.5.2.3 Bulk Erase

The following program segment demonstrates how to bulk erase the 512-byte EEPROM. The CONFIG register is not affected in this example.

```
        •
        •
        •
BULKE   LDAB    #$06
        STAB    $103B   Set to Bulk Erase Mode
        STAB    $B600   Write any Data to any EEPROM Address
        LDAB    #$07
        STAB    $103B   Turn On Programming Voltage
        JSR     DLY10   Delay 10 ms
        CLR     $103B   Turn Off High Voltage and Set to READ
                        Mode
        •
        •
        •
```

3.5.2.4 Row Erase

The following program segment demonstrates the row erase function. A ‘row’ is sixteen bytes ($B600-$B60F, $B610-$B61F... $B7F0-$B7FF). This type of erase operation saves time compared to byte erase when large sections of EEPROM are to be erased.

```
*On entry X = any address in the row to be erased
        •
        •
        •
ROWE    LDAB   #$0E
        STAB   $103B   Set to Row Erase Mode
        STAB   0,X     Write any Data to any Address in Row
        LDAB   #$0F
        STAB   $103B   Turn on High Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn Off High Voltage and Set to Read
                       Mode
        •
        •
        •
```

3.5.2.5 Byte Erase

The following program segment shows the byte erase function.

```
*On entry, X = address of byte to be erased
        •
        •
        •
BYTEE   LDAB   #$16
        STAB   $103B   Set to Byte Erase Mode
        STAB   0,X     Write any Data to the Address to Erase
        LDAB   #$17
        STAB   $103B   Turn on High Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn off High Voltage and Set to Read
                       Mode
        •
        •
        •
```

3.5.3 System Configuration Register (CONFIG)

The MC68HC11A8 can be configured to specific system requirements through the use of hardwired options such as the mode select pins, semi-permanent EEPROM control bit specifications (CONFIG register), or by use of control registers. The configuration control register (CONFIG) is implemented in EEPROM cells and controls the presence

of ROM and EEPROM in the memory map, as well as enabling the COP watchdog system. A security feature to protect data in the EEPROM and RAM is also available on mask programmed MC68HC11A8s.

	7	6	5	4	3	2	1	0	
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG
RESET	(see **3.5.3.2 Operation of the Configuration Mechanism**)								

Bits 7, 6, 5, and 4 — Not Implemented
These bits are always read as zero.

NOSEC — Security Mode Disable Bit
This bit is only implemented if it is specifically requested at the time mask ROM information is submitted. When this bit is not implemented it always reads one.
When RAM and EEPROM security are required, the NOSEC bit can be programmed to zero to enable the software anti-theft mechanism. When clear, the NOSEC bit prevents the selection of expanded multiplexed operating modes. If the MCU is reset in the special bootstrap operating mode while NOSEC is zero, EEPROM, RAM, and CONFIG are erased before the loading process continues.
0 = Enable Security Mode
1 = Disable Security Mode

NOCOP — COP System Disable
0 = COP Watchdog System Enabled
1 = COP Watchdog System Disabled

ROMON — Enable On-Chip ROM
When this bit is clear, the 8K ROM is disabled, and that memory space becomes externally accessed space. In the single-chip operating mode, the internal 8K ROM is enabled regardless of the state of the ROMON bit.

EEON — Enable On-Chip EEPROM
When this bit is clear, the 512-byte EEPROM is disabled, and that memory space becomes externally accessed space.

3.5.3.1 Programming and Erasure of the CONFIG Register

Since the CONFIG register is implemented with EEPROM cells, special provisions must be made to erase and program this register. The normal EEPROM control bits in the PPROG register are used for this purpose. Programming follows the same procedure as programming a byte in the 512-byte EEPROM except the CONFIG register address is used. Erase also follows the same procedure as that used for the EEPROM except that only bulk erase can be used on the CONFIG register. When the CONFIG register is erased, the 512-byte EEPROM array is also erased. Be sure to check the Technical Summary for the particular MC68HC11 Family member you are using.

On mask set B96D and newer, the CONFIG register may only be programmed or erased while the MCU is operating in the test mode or the bootstrap mode. This interlock was added to help prevent accidental changes to the CONFIG register.

The following program segment demonstrates how to program the CONFIG register. This program assumes that the CONFIG register was previously erased.

```
*On entry, A = data to be programmed onto CONFIG
          •
          •
          •
PROGC   LDAB   #$02
        STAB   $103B   Set EELAT Bit (EEPGM = 0)
        STAA   $103F   Store Data to CONFIG Address
        LDAB   #$03
        STAB   $103B   Turn on Programming Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn Off High Voltage and Set to READ
                       Mode
          •
          •
          •
```

The following program segment demonstrates the erase procedure for the CONFIG register.

```
          •
          •
          •
BULKC   LDAB   #$06
        STAB   $103B   Set Bulk Erase Mode
        STAB   $103F   Write any Data to CONFIG
        LDAB   #$07
        STAB   $103B   Turn on Programming Voltage
        JSR    DLY10   Delay 10 ms
        CLR    $103B   Turn Off High Voltage and Set to READ
                       Mode
          •
          •
          •
```


3.5.3.2 Operation of the Configuration Mechanism

The CONFIG register consists of an EEPROM byte and static working latches. This register controls the start-up configuration of the MCU. The contents of the EEPROM CONFIG byte are transferred into static working latches during any reset sequence. The operation of the MCU is controlled directly by these latches and not the actual EEPROM byte. Changes to the EEPROM byte do not affect operation of the MCU until after the next reset sequence. When programming the CONFIG register, the EEPROM byte is being accessed. When the CONFIG register is being read, the static latches are being accessed.

To change the value in the CONFIG register proceed as follows:

1. Erase the CONFIG register.

CAUTION

Do not issue a reset at this time.

2. Program the new value to the CONFIG register.
3. Issue a reset so the new configuration will take effect.

4 PARALLEL I/O

The MC68HC11A8 has 40 I/O pins arranged as five 8-bit ports. All of these pins serve multiple functions depending on the operating mode and data in the control registers. This section explains the operation of these pins only when they are used for parallel I/O.

Ports C and D are used as general purpose input and/or output pins under direct control of their respective data direction registers. Ports A, B, and E, with the exception of port A pin 7, are fixed direction inputs or outputs and therefore do not have data direction registers. Port B, port C, the STRA pin, and the STRB pin are used for strobed and/or handshake modes of parallel I/O, as well as general purpose I/O.

4.1 General-Purpose I/O (Ports C and D)

Each port I/O line has an associated bit in a specific port data register and port data direction register. The data direction register bits are used to specify the primary direction of data for each I/O line. When an output line is read, the value at the input to the pin driver is returned. When a line is configured as an input, that pin becomes a high-impedance input. If a write is executed to an input line, the value does not affect the I/O pin, but is stored in an internal latch. When the line becomes an output, this value appears at the I/O pin. Data direction register bits are cleared by reset to configure I/O pins as inputs.

The AS and R/$\overline{W}$ pins are dedicated to bus control while in the expanded multiplexed operating modes, or parallel I/O strobes (STRA and STRB) while in the single chip operating modes.

4.2 Fixed Direction I/O (Ports A, B, and E)

The lines for ports A, B, and E (except for port A bit 7) have fixed data directions. When port A is being used for general purpose I/O, bits 0, 1, and 2 are configured as input only and writes to these lines have no effect. Bits 3, 4, 5, and 6 of port A are configured as output only and reads of these lines return the levels sensed at the input to the line drivers. Port A bit 7 can be configured as either a general-purpose input or output using the DDRA7 bit in the pulse accumulator control register. When port B is being used for general purpose output, it is configured as output only and reads of these lines will return the levels sensed at the input of the pin drivers. Port E contains the eight A/D channel inputs, but these lines may also be used as general purpose digital inputs. Writes to the port E address have no effect.

4.3 Simple Strobed I/O

The simple strobed mode of parallel I/O is invoked and controlled by the parallel I/O control register (PIOC). This mode is selected when the handshake bit (HNDS) in the PIOC register is clear. Port C becomes a strobed input port with the STRA line as the edge-detecting latch command input. Also, port B becomes a strobed output port with the STRB line as the output strobe. The logic sense of the STRB output is selected by the invert strobe B bit (INVB) in the PIOC register.

4.3.1 Strobed Input Port C

In this mode, there are two addresses where port C may be read, the PORTC data register and the alternate latched port C register (PORTCL). The data direction register still controls the data direction of all port C lines. Even when the strobed input mode is selected, any or all of the port C lines may still be used for general purpose I/O.

The STRA line is used as an edge-detecting input, and the edge-select for strobe A (EGA) bit in the PIOC register defines either falling or rising edge as the significant edge. Whenever the selected edge is detected at the STRA pin, the current logic levels at port C lines are latched into the PORTCL register and the strobe A flag (STAF) in the PIOC register is set. If the strobe A interrupt enable (STAI) bit in PIOC is also set, an internal interrupt sequence is requested. The strobe A flag (STAF) is automatically cleared by reading the PIOC register (with STAF set) followed by a read of the PORTCL register. Data is latched in the PORTCL register whether or not the STAF flag was previously clear.

4.3.2 Strobed Output Port B

In this mode, the STRB pin is a strobe output which is pulsed for two E clock periods each time there is a write to port B. The INVB bit in the PIOC register controls the polarity of the pulse on the STRB line.

4.4 Full Handshake I/O

The full handshake modes of parallel I/O involve port C and the STRA and STRB lines. There are two basic modes (input and output) and an additional variation on the output handshake mode that allows three-stated operation of port C. In all handshake modes, STRA is an edge-detecting input, and STRB is a handshake output line.

When full input handshake protocol is specified, both general purpose input and/or general purpose output can coexist at port C. When full output handshake protocol is specified, general purpose output can coexist with the handshake outputs at port C, but the three-state feature of the output handshake mode interferes with general purpose input in two ways. First, in full output handshake, the port C lines are outputs whenever STRA is at its active level regardless of the data direction register bits. This potentially conflicts with any external device trying to drive port C unless that external device has an open-drain type output driver. Second, the value returned on reads of port C is the state of the outputs of an internal port C output latch regardless of the states of the data direction register bits, so that the data written for output handshake can be read even if the pins are in a three-state condition.

4.4.1 Input Handshake Protocol

In the input handshake protocol, port C is a latching input port, STRA is an edge-sensitive latch command from the external system that is driving port C, and STRB is a "ready" output line controlled by logic in the MCU.

When a "ready" condition is recognized, the external device places data on the port C lines, then pulses the STRA line. The active edge on the STRA line latches the port C data into the PORTCL register, sets the STAF flag (optionally causing an interrupt), and deasserts the STRB line. Deassertion of the STRB line automatically inhibits the external device from strobing new data into port C. Reading the PORTCL latch register (independent of clearing the STAF flag) asserts the STRB line, indicating that new data may now be applied to port C.

The STRB line can be configured (with the PLS control bit) to be a pulse output (pulse mode) or a static output (interlocked mode).

The port C data direction register bits should be cleared for each line that is to be used as a latched input line. However, some port C lines can be used as latched inputs with the input handshake protocol while, at the same time, using some port C lines as static inputs, and some port C lines as static outputs. The input handshake protocol has no effect on the use of port C lines as static inputs or as static outputs. Reads of the PORTC data register always return the static logic level at the port C lines (for lines configured as inputs). Writes to either the PORTC data register or the alternate latched port C register (PORTCL) send information to the same port C output register without affecting the input handshake strobes.

4.4.2 Output Handshake Protocol

In the output handshake protocol, port C is an output port, STRB is a "ready" output, and STRA is an edge-sensitive acknowledge input signal, used to indicate to the MCU that the output data has been accepted by the external device. In a variation of this output handshake protocol, STRA is also used as an output-enable input, as well as an edge-sensitive acknowledge input.

The MCU places data on the port C output lines and then indicates stable data is available by asserting the STRB line. The external device then processes the available data and pulses the STRA line to indicate that new data may be placed on the port C output lines. The active edge on the STRA line causes the STRB line to be deasserted and the STAF status flag to be set. In response to the STAF bit being set, the program transfers new data out of port C as required. Writing data to the PORTCL register causes the data to appear on port C lines and asserts the STRB line.

There is a variation to the output handshake protocol that allows three-state operation on port C. It is possible to directly connect this 8-bit parallel port to other three-state devices with no additional parts.

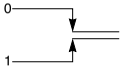
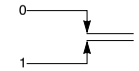
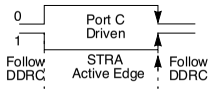
While the STRA input line is inactive, all port C lines obey the data direction specified by the data direction register so that lines which are configured as inputs are high impedance. When the STRA line is activated, all port C lines are forced to outputs regardless of the data in the data direction register. Note that in output handshake protocol, reads of port C always return the value sensed at the input to the output buffer regardless of the state of the data direction register bits because the lines would not necessarily have meaningful data on them in the three-state variation of this protocol. This operation makes it impractical to use some port C lines as static inputs, while using others as handshake outputs, but does not interfere with the use of some port C lines as static outputs. Port C lines intended as static outputs or normal handshake outputs should have their corresponding data direction register bits set, and lines intended as three-state handshake outputs should have their corresponding data direction register bits clear.

4.5 Parallel I/O Control Register (PIOC)

The parallel handshake I/O functions are available only in the single-chip operating mode. The PIOC is a read/write register except for bit 7 which is read only. **Table 4-1** shows a summary of handshake I/O operations.

Table 4-1 Handshake I/O Operations Summary

	STAI	CWOM	INVB
0	STAF Interrupts Inhibited	Port C Outputs Normal	STRB Active Low
1	STAF Interrupts Enabled	Port C Outputs Open-Drain	STRB Active High

	STAF Clearing Sequence[1]	HNDS	OIN	PLS	EGA	Port C	Port B
Simple Strobe Mode	Read PIOC with STAF = 1 then Read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA.	STRB pulses on writes to port B.
Full Input Handshake	Read PIOC with STAF = 1 then Read PORTCL	1	0	0 = STRB Active Level 1 = STRB Active Pulse		Inputs latched into PORTCL on any active edge on STRA.	Normal output port. Unaffected in handshake modes
Full Output Handshake	Read PIOC with STAF = 1 then Write to PORTCL	1	1	0 = STRB Active Level 1 = STRB Active Pulse		Driven as outputs if STRA at active level. Follows DDRC if STRA not at active level.	Normal output port. Unaffected in handshake modes

NOTE:
1. Set by active edge on STRA

	7	6	5	4	3	2	1	0	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
RESET	0	0	0	0	0	U	1	1	

STAF — Strobe A Interrupt Status Flag
This bit is set when a selected edge occurs on strobe A. Clearing it depends on the state of HNDS and OIN bits. In simple strobed mode or in full input handshake mode, STAF is cleared by reading the PIOC register with STAF set followed by reading the PORTCL register. In output handshake, STAF is cleared by reading the PIOC register with STAF set followed by writing to the PORTCL register.

STAI — Strobe A Interrupt Enable Mask
When the I bit in the condition code register is clear and STAI is set, STAF (when set) will request an interrupt.

CWOM — Port C Wire-OR Mode
CWOM affects all eight port C pins together
0 = Port C outputs are normal CMOS outputs
1 = Port C outputs act as open-drain outputs

HNDS — Handshake Mode
When clear, strobe A acts as a simple input strobe to latch data into PORTCL, and strobe B acts as a simple output strobe which pulses after a write to port B. When set, a handshake protocol involving port C, STRA, and STRB is selected (see the definition for the OIN bit).
0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshaking
This bit has no meaning when HNDS = 0.
0 = Input handshake
1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation
This bit has no meaning if HNDS = 0. When interlocked handshake operation is selected, strobe B, once activated, stays active until the selected edge of strobe A is detected. When pulsed handshake operation is selected, strobe B is pulsed for two E cycles.
0 = Interlocked handshake select
1 = Pulsed handshake selected

EGA — Active Edge for Strobe A
0 = Falling edge of STRA is selected. When output handshake is selected, port C lines obey the data direction register while STRA is low, but port C is forced to output when STRA is high.
1 = Rising edge of STRA is selected. When output handshake is selected, port C lines obey the data direction register while STRA is high, but port C is forced to output when STRA is low.

INVB — Invert Strobe B
0 = Active level is logic zero
1 = Active level is logic one

5.8.2 Serial Communications Control Register 1 (SCCR1)

The serial communications control register 1 (SCCR1) provides the control bits which: (1) determine the word length, and (2) select the method used for the wake-up feature.

	7	6	5	4	3	2	1	0	
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
RESET	U	U	0	0	0	0	0	0	

R8 — Receive Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

T8 —Transmit Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character. It is not necessary to write to this bit for every character transmitted, only when the sense is to be different than that for the previous character.

Bit 5 — Not Implemented
This bit always reads zero.

M — SCI Character Length
0 = 1 start bit, 8 data bits, 1 stop bit
1 = 1 start bit, 9 data bits, 1 stop bit

WAKE — Wake Up Method Select
0 = Idle Line
1 = Address Mark

Bits 2-0 — Not Implemented
These bits always read zero.

5.8.3 Serial Communications Control Register 2 (SCCR2)

The serial communications control register 2 (SCCR2) provides the control bits which enable/disable individual SCI functions.

	7	6	5	4	3	2	1	0	
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
RESET	0	0	0	0	0	0	0	0	

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt if TDRE = 1

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI Interrupt if TC = 1

RIE — Receive Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt if RDRF or OR = 1

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt if IDLE = 1

TE — Transmit Enable
When the transmit enable bit is set, the transmit shift register output is applied to the TxD line. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state. After loading the last byte in the serial communications data register and receiving the TDRE flag, the user can clear TE. Transmission of the last byte will then be completed before the transmitter gives up control of the TxD pin. While the transmitter is active, the data direction register control for port D bit 1 is overridden and the line is forced to be an output.

RE — Receive Enable
When the receive enable bit is set, the receiver is enabled. When RE is clear, the receiver is disabled and all of the status bits associated with the receiver (RDRF, IDLE, OR, NF, and FE) are inhibited. While the receiver is enabled, the data direction register control for port D bit 0 is overridden and the line is forced to be an input.

RWU — Receiver Wake Up
When the receiver wake-up bit is set by the user's software, it puts the receiver to sleep and enables the "wake up" function. If the WAKE bit is cleared, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If the WAKE bit is set, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send Break
If the send break bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or sending data. If SBK remains set, the transmitter will continually send whole blocks of zeros (sets of 10 or 11) until cleared. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. If the transmitter is currently empty and idle, setting and clearing SBK is likely to queue two character times of break because the first break transfers almost immediately to the shift register and the second is then queued into the parallel transmit buffer.

5.8.4 Serial Communications Status Register (SCSR)

The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt.

	7	6	5	4	3	2	1	0	
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
RESET	1	1	0	0	0	0	0	0	

TDRE — Transmit Data Register Empty
The transmit data register empty bit is set to indicate that the content of the serial communications data register have been transferred to the transmit serial shift register. This bit is cleared by reading the SCSR (with TDRE = 1) followed by a write to the SCDR.

TC — Transmit Complete
The transmit complete bit is set at the end of a data frame, preamble, or break condition if:

1. TE = 1, TDRE = 1, and no pending data, preamble, or break is to be transmitted; or
2. TE = 0, and the data, preamble, or break in the transmit shift register has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions have occurred.
The TC bit is cleared by reading the SCSR (with TC set) followed by a write to the SCDR.

RDRF — Receive Data Register Full
The receive data register full bit is set when the receiver serial shift register is transferred to the SCDR. The RDRF bit is cleared when the SCSR is read (with RDRF set) followed by a read of the SCDR.

IDLE — Idle Line Detect
The idle line detect bit, when set, indicates the receiver has detected an idle line. The IDLE bit is cleared by reading the SCSR with IDLE set followed by reading SCDR. Once the IDLE status flag is cleared, it will not be set again until after the RxD line has been active and becomes idle again.

OR — Overrun Error
The overrun error bit is set when the next byte is ready to be transferred from the receive shift register to the SCDR which is already full (RDRF bit is set). When an overrun error occurs, the data which caused the overrun is lost and the data which was already in SCDR is not disturbed. The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCDR.

NF — Noise Flag

The noise flag bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with NF set), followed by a read of the SCDR.

FE — Framing Error

The framing error bit is set when no stop bit was detected in the received data character. The FE bit is set at the same time as the RDRF is set. If the byte received causes both framing and overrun errors, the processor will only recognize the overrun error. The framing error flag inhibits further transfer of data into the SCDR until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to one) followed by a read of the SCDR.

Bit 0 — Not Implemented

This bit always reads zero.

5.8.5 Baud Rate Register (BAUD)

The baud rate register selects the different baud rates which may be used as the rate control for the transmitter and receiver. The SCP[0:1] bits function as a prescaler for the SCR[0:2] bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency.

	7	6	5	4	3	2	1	0	
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
RESET	0	0	0	0	0	U	U	U	

TCLR — Clear Baud Rate Counters (Test)

This bit is used to clear the baud rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

SCP1 and SCP0 — SCI Baud Rate Prescaler Selects

The E clock is divided by the factors shown in **Table 5-1**. This prescaled output provides an input to a divider which is controlled by the SCR2-SCR0 bits.

Table 5-1 First Prescaler Stage

SCP1	SCP0	Internal Processor Clock Divided By
0	0	1
0	1	3
1	0	4
1	1	13

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects

These three bits select the baud rates for both the transmitter and the receiver. The prescaler output described above is further divided by the factors shown in **Table 5-2**.

Table 5-2 Second Prescaler Stage

SCR2	SCR1	SCR0	Prescaler Output Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

RCKB — SCI Baud Rate Clock Check (Test)

This bit is used during factory testing to enable the exclusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

The diagram shown in **Figure 5-7** and the data given in **Table 5-3** and **Table 5-4** illustrate the divider chain used to obtain the baud rate clock. Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (Tx). The actual divider chain is controlled by the combined SCP[1:0] and SCR[2:0] bits in the baud rate register as illustrated.

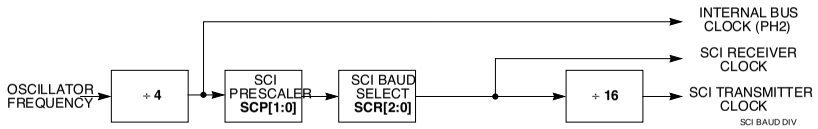


Figure 5-7 Rate Generator Division

Table 5-3 Prescaler Highest Baud Rate Frequency Output

SCP Bit 1	SCP Bit 0	Clock* Divided By	Crystal Frequency (MHz) 12.0	8.3886	8.0	4.9152	4.0	3.6864
0	0	1	187.50 K Baud	131.072 K Baud	125.000 K Baud	76.80 K Baud	62.50 K Baud	57.60 K Baud
0	1	3	62.50 K Baud	43.690 K Baud	41.666 K Baud	25.60 K Baud	20.833 K Baud	19.20 K Baud
1	0	4	46.875 K Baud	32.768 K Baud	31.250 K Baud	19.20 K Baud	15.625 K Baud	14.40 K Baud
1	1	13	14.423 K Baud	10.082 K Baud	9600 Baud	5.907 K Baud	4800 Baud	4430 Baud

*The clock in the "Clock Divided By" column is the internal processor clock

NOTE

The divided frequencies shown in **Table 5-3** represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific crystal frequency and only using the prescaler division. Lower baud rates may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

Table 5-4 Transmit Baud Rate Output for a Given Prescaler Output

SCR Bit			Divided	Representative Highest Prescaler Baud Rate Output					
2	1	0	By	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud	4800 Baud
0	0	0	1	131.072 K Baud	32.768 K Baud	76.80 K Baud	19.20 K Baud	9600 Baud	4800 Baud
0	0	1	2	65.536 K Baud	16.384 K Baud	38.40 K Baud	9600 Baud	4800 Baud	2400 Baud
0	1	0	4	32.768 K Baud	8.192 K Baud	19.20 K Baud	4800 Baud	2400 Baud	1200 Baud
0	1	1	8	16.384 K Baud	4.096 K Baud	9600 Baud	2400 Baud	1200 Baud	600 Baud
1	0	0	16	8.192 K Baud	2.048 K Baud	4800 Baud	1200 Baud	600 Baud	300 Baud
1	0	1	32	4.096 K Baud	1.024 K Baud	2400 Baud	600 Baud	300 Baud	150 Baud
1	1	0	64	2.048 K Baud	512 Baud	1200 Baud	300 Baud	150 Baud	75 Baud
1	1	1	128	1.024 K Baud	256 Baud	600 Baud	150 Baud	75 Baud	—

NOTE

Table 5-4 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The five examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.

7 ANALOG-TO-DIGITAL CONVERTER

The MC68HC11A8 includes an 8-channel, multiplexed-input, successive approximation, analog-to-digital (A/D) converter with sample and hold to minimize conversion errors caused by rapidly changing input signals. Two dedicated lines (V_{RL}, V_{RH}) are provided for the reference voltage inputs. These pins may be connected to a separate or isolated power supply to ensure full accuracy of the A/D conversion. The 8-bit A/D converter has a total error of ±1 LSB which includes ± 1/2 LSB of quantization error and accepts analog inputs which range from V_{RL} to V_{RH}. Smaller analog input ranges can also be obtained by adjusting V_{RH} and V_{RL} to the desired upper and lower limits. Conversion is specified and tested for V_{RL} = 0 V and V_{RH} = 5 V ± 10%; however, laboratory characterization over the full temperature range indicates little or no degradation with V_{RH}-V_{RL} as low as 2.5 to 3 V. The A/D system can be operated with V_{RH} below V_{DD} and/or V_{RL} above V_{SS} as long as V_{RH} is above V_{RL} by enough to support the conversions (2.5 to 5.0 V). Each conversion is accomplished in 32 MCU E clock cycles, provided the E clock rate is greater than 750 kHz. For systems which operate at clock rates less than 750 kHz, an internal R-C oscillator must be used to clock the A/D system. The internal R-C oscillator is selected by setting the CSEL bit in the OPTION register.

NOTE

Only four A/D input channels are available in the 48-pin version.

7.1 Conversion Process

The A/D converter is ratiometric. An input voltage equal to V_{RL} converts to $00 and an input voltage equal to V_{RH} converts to $FF (full scale), with no overflow indication. For ratiometric conversions, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{RL}.

Figure 7-1 shows the detailed sequence for a set of four conversions. This sequence begins one E clock cycle after a write to the A/D control/status register (ADCTL). **Figure 7-2** shows a model of the port E A/D channel inputs. This model is useful for understanding the effects of external circuitry on the accuracy of A/D conversions.

7.2 Channel Assignments

A multiplexer allows the single A/D converter to select one of sixteen analog signals. Eight of these channels correspond to port E input lines to the MCU, four of the channels are for internal reference points or test functions, and four channels are reserved for future use. **Table 7-1** shows the signals selected by the four channel select control bits.

7.3 Single-Channel Operation

There are two variations of single-channel operation. In the first variation (SCAN = 0), the single selected channel is converted four consecutive times with the first result being stored in A/D result register 1 (ADR1) and the fourth result being stored in register ADR4. After the fourth conversion is complete, all conversion activity is halted until a new conversion command is written to the ADCTL register. In the second variation (SCAN = 1), conversions continue to be performed on the selected channel with the fifth conversion being stored in register ADR1 (overwriting the first conversion result), the sixth conversion overwrites ADR2, and so on.

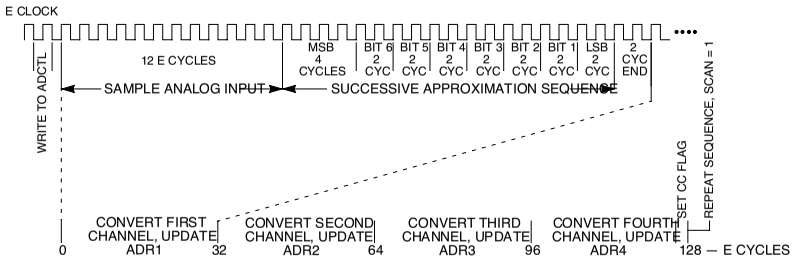
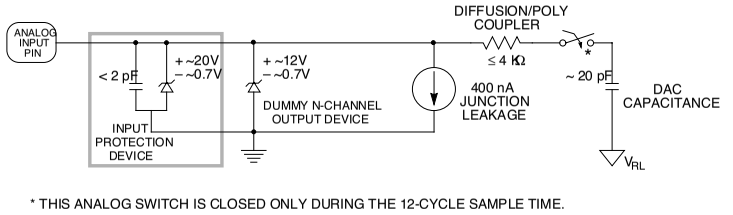


Figure 7-1 A/D Conversion Sequence



* THIS ANALOG SWITCH IS CLOSED ONLY DURING THE 12-CYCLE SAMPLE TIME.

Figure 7-2 A/D Pin Model

7.4 Multiple-Channel Operation

There are two variations in multiple-channel operation. In the first variation (SCAN = 0), the selected group of four channels are converted, one time each, with the first result being stored in register ADR1 and the fourth result being stored in register ADR4. After the fourth conversion is complete, all conversion activity is halted until a new conversion command is written to the ADCTL register. In the second variation (SCAN = 1), conversions continue to be performed on the selected group of channels with the fifth conversion being stored in register ADR1 (replacing the earlier conversion result for the first channel in the group), the sixth conversion overwrites ADR2, and so on.

7.5 Operation in STOP and WAIT Modes

If a conversion sequence is still in process when either the STOP or WAIT mode is entered, the conversion of the current channel is suspended. When the MCU resumes normal operation, that channel will be re-sampled and the conversion sequence resumed. As the MCU exits the WAIT mode, the A/D circuits are stable and valid results can be obtained on the first conversion. However, in STOP mode, all analog bias currents are disabled and it becomes necessary to allow a stabilization period when leaving the STOP mode. If the STOP mode is exited with a delay, there will be enough time for these circuits to stabilize before the first conversion. If the STOP mode is exited with no delay (DLY bit in OPTION register equal to zero), sufficient time must be allowed for the A/D circuitry to stabilize to avoid invalid results (see **7.8 A/D Power-Up and Clock Select**).

7.6 A/D Control/Status Register (ADCTL)

All bits in this register may be read or written, except bit 7 which is a read-only status indicator and bit 6 which always reads as a zero.

	7	6	5	4	3	2	1	0	
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
RESET	0	0	U	U	U	U	U	U	

CCF — Conversions Complete Flag
This read-only status indicator is set when all four A/D result registers contain valid conversion results. Each time the ADCTL register is written, this bit is automatically cleared to zero and a conversion sequence is started. In the continuous modes, conversions continue in a round-robin fashion and the result registers continue to be updated with current data even though the CCF bit remains set.

NOTE

The user must write to register ADCTL to initiate conversion. To abort a conversion in progress, write to the ADCTL register and a new conversion sequence is initiated immediately.

Bit 6 — Not Implemented
This bit always reads zero.

SCAN — Continuous Scan Control
When this control bit is clear, the four requested conversions are performed once to fill the four result registers. When this control bit is set, conversions continue in a round-robin fashion with the result registers being updated as data becomes available.

MULT — Multiple-Channel/Single Channel Control
When this bit is clear, the A/D system is configured to perform four consecutive conversions on the single channel specified by the four channel select bits CD through CA (bits [3:0] of the ADCTL register). When this bit is set, the A/D system is configured to perform a conversion on each of four channels where each result register corresponds to one channel.

CAUTION

When the multiple channel continuous scan mode is used, extra care is needed in the design of circuitry driving the A/D inputs. Refer to the A/D Pin Model and A/D Conversion Sequence figures in addition to the following discussion. The charge on the capacitive DAC array prior to the sample time is related to the voltage on the previously converted channel. A charge share situation exists between the internal DAC capacitance and the external circuit capacitance. Although the amount of charge involved is small the rate at which it is repeated is every 64 microseconds for an E clock of 2 MHz. The RC charging rate of the external circuit must be balanced against this charge sharing effect to avoid accuracy errors.

CD — Channel Select D
CC — Channel Select C
CB — Channel Select B
CA — Channel Select A

These four bits are used to select one of 16 A/D channels (see **Table 7-1**). When a multiple channel mode is selected (MULT = 1), the two least-significant channel select bits (CB and CA) have no meaning and the CD and CC bits specify which group of four channels are to be converted. The channels selected by the four channel select control bits are shown in **Table 7-1**.

Table 7-1 Analog-to-Digital Channel Assignments

CD	CC	CB	CA	Channel Signal	Result in ADRx if MULT=1
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4*	ADR1
0	1	0	1	AN5*	ADR2
0	1	1	0	AN6*	ADR3
0	1	1	1	AN7*	ADR4
1	0	0	0	Reserved	ADR1
1	0	0	1	Reserved	ADR2
1	0	1	0	Reserved	ADR3
1	0	1	1	Reserved	ADR4
1	1	0	0	V_{RH} Pin**	ADR1
1	1	0	1	V_{RL} Pin**	ADR2
1	1	1	0	$(V_{RH})/2$**	ADR3
1	1	1	1	Reserved**	ADR4

*Not available in 48-pin package versions.
**This group of channels used during factory test.

7.7 A/D Result Registers 1, 2, 3, and 4 (ADR1, ADR2, ADR3, and ADR4)

The A/D result registers are read-only registers used to hold an 8-bit conversion result. Writes to these registers have no effect. Data in the A/D result registers is valid when the CCF flag bit in the ADCTL register is set, indicating a conversion sequence is complete. If conversion results are needed sooner refer to **Figure 7-1**. For example the ADR1 result is valid 33 cycles after an ADCTL write. Refer to the A/D channel assignments in **Table 7-1** for the relationship between the channels and the result registers.

7.8 A/D Power-Up and Clock Select

A/D power-up is controlled by bit 7 (ADPU) of the OPTION register. When ADPU is cleared, power to the A/D system is disabled. When ADPU is set, the A/D system is enabled. A delay of as much as 100 microseconds is required after turning on the A/D converter to allow the analog bias voltages to stabilize.

Clock select is controlled by bit 6 (CSEL) of the OPTION register. When CSEL is cleared, the A/D system uses the system E clock. When CSEL is set, the A/D system uses an internal R-C clock source, which runs at about 1.5 MHz. The MCU E clock is not suitable to drive the A/D system if it is operating below 750 kHz, in which case the R-C internal clock should be selected. A delay of 10 ms is required after changing CSEL from zero to one to allow the R-C oscillator to start and internal bias voltages to settle. Refer to **9.1.5 Configuration Options Register (OPTION)** for additional information. Note that the CSEL control bit also enables a separate R-C oscillator to drive the EEPROM charge pump.

When the A/D system is operating with the MCU E clock, all switching and comparator operations are synchronized to the MCU clocks. This allows the comparator results to be sampled at quiet clock times to minimize noise errors. The internal R-C oscillator is asynchronous to the MCU clock so noise will affect A/D results more while CSEL = 1.

8 PROGRAMMABLE TIMER, RTI, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 Programmable Timer

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU E clock. Input functions are called input captures. These input captures record the count from the free-running counter in response to a detected edge on an input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has three input capture registers and five output compare registers.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFF8 regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.

The result obtained by an input capture corresponds to the value of the counter one E clock cycle after the transition which triggered the edge-detection logic. The selected edge transition sets the ICxF bit in timer interrupt flag register 1 (TFLG1) and can cause an interrupt if the corresponding ICxI bit(s) is (are) set in the timer interrupt mask register 1 (TMSK1). A read of the input capture register's most significant byte inhibits captures for one E cycle to allow a double-byte read of the full 16-bit register.

8.1.3 Output Compare

All output compare registers are 16-bit read/write registers which are initialized to $FFFF by reset. They can be used as output waveform controls or as elapsed time indicators. If an output compare register is not used, it may be used as a storage location.

All output compare registers have a separate dedicated comparator for comparing against the free-running counter. If a match is found, the corresponding output compare flag (OCxF) bit in TFLG1 is set and a specified action is automatically taken. For output compare functions two through five the automatic action is controlled by pairs of bits (OMx and OLx) in the timer control register 1 (TCTL1). Each pair of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. The output action is taken on each successful compare regardless of whether or not the OCxF flag was previously clear.

An interrupt can also accompany a successful output compare, provided that the corresponding interrupt enable bit (OCxI) is set in TMSK1.

After a write cycle to the most significant byte, output compares are inhibited for one E cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double-byte write instruction should be used in order to take advantage of the compare inhibit feature.

Writes can be made to either byte of the output compare register without affecting the other byte.

A write-only register, timer compare force (CFORC), allows forced compares. Five of the bit positions in the CFORC register correspond to the five output compares. To force a compare, or compares, a write is done to CFORC register with the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there was a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. Output actions are synchronized to the prescaled timer clock so there could be as much as 16 E clock cycles of delay between the write to CFORC and the output action.

8.1.4 Output Compare 1 I/O Pin Control

Unlike the other four output compares, output compare 1 can automatically affect any or all of the five output pins (bits 3-7) in port A as a result of a successful compare between the OC1 register and the 16-bit free-running counter. The two 5-bit registers used in conjunction with this function are the output compare 1 mask register (OC1M) and the output compare 1 data register (OC1D).

Register OC1M is used to specify the bits of port A (I/O and timer port) which are to be affected as a result of a successful OC1 compare. Register OC1D is used to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare. If an OC1 compare and another output compare occur during the same E cycle and both attempt to alter the same port A line, the OC1 compare prevails.

This function allows control of multiple I/O pins automatically with a single output compare.

Another intended use for the special I/O pin control on output compare 1 is to allow more than one output compare to control a single I/O pin. This allows pulses as short as one E clock cycle to be generated.

8.1.5 Timer Compare Force Register (CFORC)

The timer compare force register is used to force early output compare actions. The CFORC register is an 8-bit write-only register. Reads of this location have no meaning and always return logic zeros. Note that the compare force function is not generally recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undesirable operation.

	7	6	5	4	3	2	1	0	
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
RESET	0	0	0	0	0	0	0	0	

FOC1-FOC5 — Force Output Compare x Action

0 = Has no meaning

1 = Causes action programmed for output compare x, except the OCxF flag bit is not set.

Bits 2-0 — Not Implemented

These bits always read zero.

8.1.6 Output Compare 1 Mask Register (OC1M)

This register is used in conjunction with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1M register correspond bit-for-bit with the lines of port A (lines 7 through 3 only). For each bit that is affected by the successful compare, the corresponding bit in OC1M should be set to one.

Note that the pulse accumulator function shares line 7 of port A. If the DDRA7 bit in the pulse accumulator control register (PACTL) is set, then port A line 7 is configured as an output and OC1 can obtain access by setting OC1M bit 7. In this condition if the PAEN bit in the PACTL register is set, enabling the pulse accumulator input, then OC1 compares cause a write of OC1D bit 7 to an internal latch, and the output of that latch drives the pin and the pulse accumulator input. This action can then cause the pulse accumulator to take the appropriate action (pulse count or gate modes).

8.1.7 Output Compare 1 Data Register (OC1D)

This register is used in conjunction with output compare 1 to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare.

	7	6	5	4	3	2	1	0	
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
RESET	0	0	0	0	0	0	0	0	

The bits of the OC1D register correspond bit-for-bit with the lines of port A (lines 7 thru 3 only). When a successful OC1 compare occurs, for each bit that is set in OC1M, the corresponding data bit in OC1D is stored in the corresponding bit of port A. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E cycle with both attempting to alter the same port A line, the OC1 action prevails.

8.1.8 Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0	
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
RESET	0	0	0	0	0	0	0	0	

OM2, OM3, OM4, and OM5 — Output Mode

OL2, OL3, OL4, and OL5 — Output Level

These two control bits (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

OMx	OLx	Action Taken Upon Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

8.1.9 Timer Control Register 2 (TCTL2)

	7	6	5	4	3	2	1	0	
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
RESET	0	0	0	0	0	0	0	0	

Bits 7-6 — Not Implemented
These bits always read zero.

EDGxB and EDGxA — Input Capture x Edge Control.
These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x as follows:

EDGxB	EDBxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any (rising or falling) edge

8.1.10 Timer Interrupt Mask Register 1 (TMSK1)

	7	6	5	4	3	2	1	0	
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
RESET	0	0	0	0	0	0	0	0	

OCxI — Output Compare x Interrupt
If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

ICxI — Input Capture x Interrupt
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

8.1.11 Timer Interrupt Flag Register 1 (TFLG1)

Timer interrupt flag register 1 is used to indicate the occurrence of timer system events, and together with the TMSK1 register allows the timer subsystem to operate in a polled or interrupt driven system. For each bit in TFLG1, there is a corresponding bit in TMSK1 in the same bit position. If the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

These timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

	7	6	5	4	3	2	1	0	
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
RESET	0	0	0	0	0	0	0	0	

OCxF — Output Compare x Flag
This flag bit is set each time the timer counter matches the output compare register x value. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

ICxF — Input Capture x Flag
This flag is set each time a selected active edge is detected on the ICx input line. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

8.1.12 Timer Interrupt Mask Register 2 (TMSK2)

Timer interrupt mask register 2 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in timer interrupt flag register 2. In addition, two timer prescaler bits are included in this register. For each of the four most significant bits in timer flag register 2, (TFLG2), there is a corresponding bit in the timer mask register 2 (TMSK2) in the same bit position.

	7	6	5	4	3	2	1	0	
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
RESET	0	0	0	0	0	0	0	0	

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF = 1

RTII — RTI Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF = 1

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF = 1

PAII — Pulse Accumulator Input Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF = 1

Bits 3 and 2 — Not Implemented
These bits always read zero.

PR1 and PR0 — Timer Prescaler Selects

These two bits may be read at any time but may only be written during initialization. Writes are disabled after the first write or after 64 E cycles out of reset. If the MCU is in special test or special bootstrap mode, then these two bits may be written any time.

These two bits specify the timer prescaler divide factor.

PR1	PR0	Prescaler
0	0	÷ 1
0	1	÷ 4
1	0	÷ 8
1	1	÷ 16

8.1.13 Timer Interrupt Flag Register 2 (TFLG2)

Timer interrupt flag register 2 is used to indicate the occurrence of timer system events and, together with the TMSK2 register, allows the timer subsystems to operate in a polled or interrupt driven system. For each bit in timer flag register 2 (TFLG2), there is a corresponding bit in timer mask register 2 (TMSK2) in the same bit position. If the enable bit is set each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

The timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

	7	6	5	4	3	2	1	0	
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
RESET	0	0	0	0	0	0	0	0	

TOF — Timer Overflow

This bit is cleared by reset. It is set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. This bit is cleared by a write to the TFLG2 register with bit 7 set.

RTIF — Real Time Interrupt Flag

This bit is set at each rising edge of the selected tap point. This bit is cleared by a write to the TFLG2 register with bit 6 set.

PAOVF — Pulse Accumulator Overflow Interrupt Flag

This bit is set when the count in the pulse accumulator rolls over from $FF to $00. This bit is cleared by a write to the TFLG2 register with bit 5 set.

PAIF — Pulse Accumulator Input Edge Interrupt Flag

This bit is set when an active edge is detected on the PAI input pin. This bit is cleared by a write to the TFLG2 register with bit 4 set.

Bits 3-0 — Not Implemented

These bits always read zero.

8.2 Real-Time Interrupt

The real-time interrupt feature on the MCU is configured and controlled by using two bits (RTR1 and RTR0) in the PACTL register to select one of four interrupt rates. The RTII bit in the TMSK2 register enables the interrupt capability. Every timeout causes the RTIF bit in TFLG2 to be set, and if RTII is set, an interrupt request is generated. After reset, one entire real time interrupt period elapses before the RTIF flag is set for the first time.

8.3 Pulse Accumulator

The pulse accumulator is an 8-bit read/write counter which can operate in either of two modes (external event counting or gated time accumulation) depending on the state of the PAMOD control bit in the PACTL register. In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is E clock divided by two. In the gated time accumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only while the external PAI input pin is enabled.

The pulse accumulator uses port A bit 7 as its PAI input, but this pin also shares function as a general purpose I/O pin and as a timer output compare pin. Normally port A bit 7 would be configured as an input when being used for the pulse accumulator. Note that even when port A bit 7 is configured for output, this pin still drives the input to the pulse accumulator.

8.3.1 Pulse Accumulator Control Register (PACTL)

Four bits in this register are used to control an 8-bit pulse accumulator system and two other bits are used to select the rate for the real time interrupt system.

	7	6	5	4	3	2	1	0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL
RESET	0	0	0	0	0	0	0	0	

DDRA7 — Data Direction for Port A Bit 7

0 = Input only
1 = Output

PAEN — Pulse Accumulator System Enable

0 = Pulse accumulator off
1 = Pulse accumulator on

PAMOD — Pulse Accumulator Mode
0 = External event counting
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
This bit has different meanings depending on the state of the PAMOD bit.

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A zero on PAI Inhibits Counting
1	1	A one on PAI Inhibits Counting

Bits 3-2 — Not Implemented
These bits always read zero.

RTR1 and RTR0 — RTI Interrupt Rate Selects
These two bits select one of four rates for the real time periodic interrupt circuit (see **Table 8-1**). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

Table 8-1 Real Time Interrupt Rate versus RTR1 and RTR0

RTR1	RTR0	Rate	XTAL = 12.0 MHz	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	$2^{13} \div E$	8.192 ms	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	$2^{14} \div E$	16.384 ms	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	$2^{15} \div E$	32.768 ms	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	$2^{16} \div E$	65.536 ms	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

of reset. The DLY control bit is set to specify that an oscillator start-up delay is imposed upon recovery from STOP mode. The clock monitor system is disabled by CME equal zero.

9.1.3 Computer Operating Properly (COP) Reset

The MCU includes a computer operating properly watchdog system to help protect against software failures. To use a COP watchdog timer, a watchdog timer reset sequence must be executed on a regular periodic basis so that the watchdog timer is never allowed to time out.

The internal COP function includes special control bits which permit specification of one of four time out periods and even allows the function to be disabled completely. The COP system has a separate reset vector.

The NOCOP control bit, which determines whether or not a watchdog timeout causes a system reset, is implemented in an EEPROM cell in the CONFIG register. Once programmed, this bit remains set (or cleared) even when no power is applied, and the COP function is enabled or disabled independent of resident software. The NOCOP control bit may be preempted while in special modes to prevent the COP system from causing a hardware reset.

Two other control bits in the OPTION register select one of four timeout durations for the COP timer. The actual timeout period is dependent on the system E clock frequency, but for reference purposes, **Table 9-1** shows the relationship between the CR1 and CR0 control bits and the COP timeout period for various system clock frequencies.

Table 9-1 COP Timeout Period versus CR1 and CR0

CR1	CR0	Rate	XTAL = 12.0 MHz Timeout –0/+10.9 ms	XTAL = 2^{23} Timeout – 0/+15.6 ms	XTAL = 8.0 MHz Timeout – 0/+16.4 ms	XTAL = 4.9152 MHz Timeout – 0/+26.7 ms	XTAL = 4.0 MHz Timeout – 0/+32.8 ms	XTAL = 3.6864 MHz Timeout – 0/+35.6 ms
0	0	$2^{15} \div E$	10.923 ms	15.625 ms	16.384 ms	26.667 ms	32.768 ms	35.556 ms
0	1	$2^{17} \div E$	43.691 ms	62.5 ms	65.536 ms	106.67 ms	131.07 ms	142.22 ms
1	0	$2^{19} \div E$	174.76 ms	250 ms	262.14 ms	426.67 ms	524.29 ms	568.89 ms
1	1	$2^{21} \div E$	699.05 ms	1 s	1.049 s	1.707 s	2.1 s	2.276 s
		E =	**3.0 MHz**	**2.1 MHz**	**2.0 MHz**	**1.2288 MHz**	**1.0 MHz**	**921.6 kHz**

The default reset condition of the CR1 and CR0 bits is cleared which corresponds to the shortest timeout period.

The sequence required to reset the watchdog timer is:

1. Write $55 to the COP reset register (COPRST) at $103A, followed by
2. Write $AA to the same address.

Both writes must occur in correct order prior to timeout but, any number of instructions may be executed between the writes. The elapsed time between adjacent software reset sequences must never be greater than the COP time out period. Reading the COPRST register does not return meaningful data and does not affect the watchdog timer.

9.1.4 Clock Monitor Reset

The clock monitor function is enabled by the CME control bit in the OPTION register. When CME is clear, the monitor function is disabled. When the CME bit is set, the clock monitor function detects the absence of an E clock for more than a certain period of time. The timeout period is dependent on processing parameters and will be between 5 and 100 microseconds. This means that an E-clock rate of 200 kHz or more will never cause a clock monitor failure and an E-clock rate of 10 kHz or less will definitely cause a clock monitor failure. This implies that systems operating near or below an E-clock rate of 200 kHz should not use the clock monitor function.

Upon detection of a slow or absent clock, the clock monitor circuit will cause a system reset. This reset is issued to the external system via the bidirectional $\overline{\text{RESET}}$ pin. The clock monitor system has a separate reset vector.

Special considerations are needed when using a STOP function and clock monitor in the same system. Since the STOP function causes the clocks to be halted, the clock monitor function will generate a reset sequence if it is enabled at the time the STOP mode is entered.

The clock monitor is useful as a backup for the COP watchdog timer. Since the watchdog timer requires a clock to function, it will not indicate any failure if the system clocks fail. The clock monitor would detect such a failure and force the MCU to its reset state. Note that clocks are not required for the MCU to reach its reset configuration, although clocks are required to sequence through reset back to the run condition.

9.1.5 Configuration Options Register (OPTION)

This is a special purpose 8-bit register that is used (optionally) during initialization to configure internal system configuration options. With the exception of bits 7, 6, and 3 (ADPU, CSEL, and CME) which may be read or written at any time, this register may be written to only once after a reset and thereafter is a read-only register. If no write is performed to this location within 64 E-clock cycles after reset, then bits 5, 4, 1, and 0 (IRQE, DLY, CR1, and CR0) will become read-only to minimize the possibility of any accidental changes to the system configuration (writes will be ignored). While in special test modes, the protection mechanism on this register is preempted and all bits in the OPTION register may be written repeatedly.

	7	6	5	4	3	2	1	0	
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
RESET	0	0	0	1	0	0	0	0	

ADPU — A/D Power-up

This bit controls operations of the on-chip analog-to-digital converter. When ADPU is clear, the A/D system is powered down and conversion requests will not return meaningful information. To use the A/D system, this bit should be set. A 100 microsecond delay is required after ADPU is turned on to allow the A/D system to stabilize.

CSEL — A/D/EE Charge Pump Clock Source Select

This bit determines the clocking source for the on-chip A/D and EEPROM charge pump. When this bit is zero, the MCU E clock drives the A/D system and the EEPROM charge pump. When CSEL is one, on-chip separate R-C oscillators are enabled and clock the systems at about 2 MHz. When running with an E clock below 1 MHz, CSEL must be high to program or erase EEPROM. When operating below 750 kHz E clock rate, CSEL should be high for A/D conversions. A delay of 10 milliseconds is required after CSEL is turned on to allow the A/D system to stabilize.

IRQE — IRQ Edge/Level Sensitive

This bit may only be written under special circumstances as described above. When this bit is clear, the $\overline{IRQ}$ pin is configured for level sensitive wired-OR operation (low level) and when it is set, the $\overline{IRQ}$ pin is configured for edge-only sensitivity (falling edges).

DLY — STOP Exit Turn-On Delay

This bit may only be written under special circumstances as described above. This bit is set during reset and controls whether or not a relatively long turn-on delay will be imposed before processing can resume after a STOP period. If an external clock source is supplied this delay can be inhibited so that processing can resume within a few cycles of a wake up from STOP mode. When DLY is set, a 4064 E clock cycle delay is imposed to allow oscillator stabilization and when DLY is clear, this delay is bypassed.

CME — Clock Monitor Enable

This control bit may be read or written at any time and controls whether or not the internal clock monitor circuit will trigger a reset sequence when a slow or absent system clock is detected. When it is clear, the clock monitor circuit is disabled and when it is set, the clock monitor circuit is enabled. Systems operating at or below 200 kHz should not use the clock monitor function. Reset clears the CME bit.

Bit 2 — Not Implemented

This bit always reads zero.

CR1 and CR0 — COP Timer Rate Selects

These bits may only be written under special circumstances as described above. Refer to **Table 9-1** for the relationship between CR1:CR0 and the COP timeout period.

9.2 Interrupts

When an external or internal (hardware) interrupt occurs, the interrupt is not serviced until the current instruction being executed is completed. Until the current instruction is complete, the interrupt is considered pending. After completion of current instruction execution, unmasked interrupts may be serviced in accordance with an established fixed hardware priority circuit; however, one l-bit related interrupt source may be dynamically elevated to the highest I bit priority position in the hierarchy (see **9.2.5 Highest Priority I Interrupt Register (HPRIO)**).

Seventeen hardware interrupts and one software interrupt (excluding reset type interrupts) can be generated from all of the possible sources. The interrupts can be divided into two basic categories, maskable and non-maskable. In the MC68HC11A8 fifteen of the interrupts can be masked using the condition code register I bit. In addition to being maskable by the I bit in the condition code register, all of the on-chip interrupt sources are individually maskable by local control bits.

Table 9-2 IRQ Vector Interrupts

Interrupt Cause	Local Mask
External Pin	None
Parallel I/O Handshake	STAI

The software interrupt (SWI instruction) is a non-maskable instruction rather than a maskable interrupt source. The illegal opcode interrupt is a non-maskable interrupt. The last interrupt source, external input to the $\overline{XIRQ}$ pin, is considered a non-maskable interrupt because once enabled, it cannot be masked by software; however, it is masked during reset and upon receipt of an interrupt at the $\overline{XIRQ}$ pin. **Table 9-2**, **Table 9-3**, and **Table 9-4** provide a list of each interrupt, its vector location in memory, and the actual condition code and control bits that mask it. A discussion of the various interrupts is provided below. **Figure 9-3** shows the interrupt stacking order.

Table 9-3 Interrupt Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1	Reserved	—	—
•	•		
•	•		
FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	See Table 9-3
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Output Compare 5	I Bit	OC5I
FFE2, E3	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	OC3I
FFEC, ED	Timer Input Capture 2	I Bit	OC2I
FFEE, EF	Timer Input Capture 1	I Bit	OC1I
FFF0, F1	Real Time Interrupt	I Bit	RTII
FFF2, F3	$\overline{IRQ}$ (External Pin or Parallel I/O)	I Bit	See Table 9-4
FFF4, F5	$\overline{XIRQ}$ Pin (Pseudo Non-Maskable Interrupt)	X Bit	None
FFF6, F7	SWI	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure (Reset)	None	NOCOP
FFFC, FD	COP Clock Monitor Fail (Reset)	None	CME
FFFE, FF	$\overline{RESET}$	None	None

Table 9-4 SCI Serial System Interrupts

Interrupt Cause	Local Mask
Receive Data Register Full	RIE
Receiver Overrun	RIE
Idle Line Detect	ILIE
Transmit Data Register Empty	TIE
Transmit Complete	TCIE

9.2.1 Software Interrupt (SWI)

The software interrupt is executed in the same manner as any other instruction and will take precedence over interrupts only if the other interrupts are masked (I and X bits in the condition code register set). The SWI instruction is executed in a manner similar to other maskable interrupts in that it sets the I bit, CPU registers are stacked, etc.

NOTE

The SWI instruction will not be fetched if an interrupt is pending. However, once an SWI instruction has begun, no interrupt can be honored until the SWI vector has been fetched.

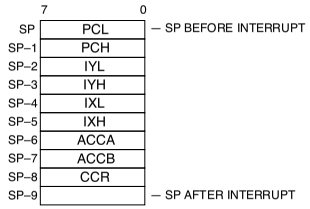


Figure 9-3 Interrupt Stacking Order

9.2.2 Illegal Opcode Trap

Since not all possible opcodes or opcode sequences are defined, an illegal opcode detection circuit has been included. When an illegal opcode is detected, an interrupt is requested to the illegal opcode vector. The illegal opcode vector should never be left uninitialized. It is a good idea to reinitialize the stack pointer as a result of an illegal opcode interrupt so repeated execution of illegal opcodes does not cause stack overruns.

9.2.3 Interrupt Mask Bits in Condition Code Register

Upon reset, both the X bit and the I bit are set to inhibit all maskable interrupts and $\overline{\text{XIRQ}}$. After minimum system initialization, software may clear the X bit by a TAP instruction, thus enabling $\overline{\text{XIRQ}}$ interrupts. Thereafter software cannot set the X bit so an $\overline{\text{XIRQ}}$ interrupt is effectively a nonmaskable interrupt. Since the operation of the I

bit related interrupt structure has no effect on the X bit, the external $\overline{\text{XIRQ}}$ pin remains effectively non-masked. In the interrupt priority logic, the $\overline{\text{XIRQ}}$ interrupt is a higher priority than any source that is maskable by the I bit. All I bit related interrupts operate normally with their own priority relationship. When an I bit related interrupt occurs, the I bit is automatically set by hardware after stacking the condition code register byte, but the X bit is not affected. When an X bit related interrupt occurs, both the X bit and the I bit are automatically set by hardware after stacking the condition code register. An RTI (return from interrupt) instruction restores the X and I bits to their pre-interrupt request state.

9.2.4 Priority Structure

Interrupts obey a fixed hardware priority circuit to resolve simultaneous requests; however, one I bit related interrupt source may be elevated to the highest I bit priority position in the resolution circuit. The first six interrupt sources are not masked by the I bit in the condition code register and have the fixed priority interrupt relationship of: reset, clock monitor fail, COP fail, illegal opcode, and $\overline{\text{XIRQ}}$. (SWI is actually an instruction and has highest priority other than reset in the sense that once the SWI opcode is fetched, no other interrupt can be honored until the SWI vector has been fetched). Each of these sources is an input to the priority resolution circuit. The highest I bit masked priority input to the resolution circuit is assigned under software control (of the HPRIO register) to be connected to any one of the remaining I bit related interrupt sources. In order to avoid timing races, the HPRIO register may only be written while the I bit related interrupts are inhibited (I bit in condition code register is a logic one). An interrupt that is assigned to this high priority position is still subject to masking by any associated control bits or the I bit in the condition code register. The interrupt vector address is not affected by assigning a source to this higher priority position.

Figure 9-4, **Figure 9-5**, and **Figure 9-6** illustrate the interrupt process as it relates to normal processing. **Figure 9-4** shows how the CPU begins from a reset and how interrupt detection relates to normal opcode fetches. **Figure 9-5** is an expansion of a block in **Figure 9-4** and shows how interrupt priority is resolved. **Figure 9-6** is an expansion of the SCI interrupt block in **Figure 9-5**. **Figure 9-6** shows the resolution of interrupt sources within the SCI subsystem.

9.2.5 Highest Priority I Interrupt Register (HPRIO)

This register is used to select one of the I bit related interrupt sources to be elevated to the highest I bit masked position in the priority resolution circuit. In addition, four miscellaneous system control bits are included in this register.

	7	6	5	4	3	2	1	0	
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
RESET	—	—	—	—	0	1	0	1	

RBOOT — Read Bootstrap ROM

The read bootstrap ROM bit only has meaning when the SMOD bit is a one (special bootstrap mode or special test mode). At all other times, this bit is clear and may not be written.

When set, upon reset in bootstrap mode only, the small bootstrap loader program is enabled. When clear, by reset in the other three modes, this ROM is disabled and accesses to this area are treated as external accesses.

SMOD — Special Mode

The special mode bit reflects the inverse of the MODB input pin at the rising edge of reset. It is set if the MODB pin is low during reset. If MODB is high during reset, it is cleared. This bit may be cleared under software control from the special modes, thus, changing the operating mode of the MCU, but may never be set by software.

MDA — Mode Select A

The mode select A bit reflects the status of the MODA input pin at the rising edge of reset. While the SMOD bit is set (special bootstrap or special test mode in effect) the MDA bit may be written, thus, changing the operating mode, of the MCU. When the SMOD bit is clear, the MDA bit is a read-only bit and the operating mode cannot be changed without going through a reset sequence.

Table 9-5 summarizes the relationship between the SMOD and MDA bits and the MODB and MODA input pins at the rising edge of reset.

Table 9-5 Mode Bits Relationship

Inputs		Mode Description	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	Single Chip	0	0
1	1	Expanded Multiplexed	0	1
0	0	Special Bootstrap	1	0
0	1	Special Test	1	1

1 = Logic High 0 = Logic Low

IRV — Internal Read Visibility

The internal read visibility bit is used in the special modes (SMOD = 1) to affect visibility of internal reads on the expansion data bus. IRV is writeable only if SMOD = 1 and returns to zero if SMOD = 0. If IRV is clear, visibility of internal reads is blocked. If the bit is set, internal reads are visible on the external bus.

PSEL3, PSEL2, PSEL1, and PSEL0 — Priority Select

These four priority select bits are used to specify one I bit related interrupt source which becomes the highest priority I bit related source (**Table 9-6**). These bits may be written only while the I bit in CCR = 1 (interrupts masked).

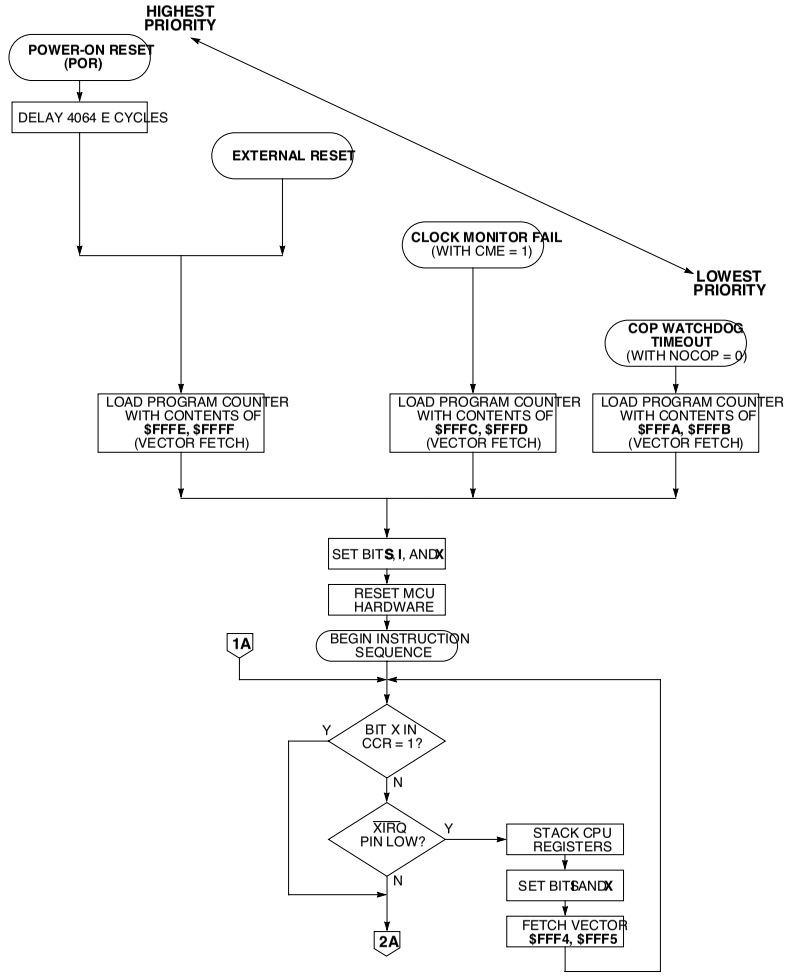


Figure 9-4 Processing Flow Out of Resets (Sheet 1 of 2)

Table 9-6 Highest Priority I Interrupt versus PSEL[3:0]

PSEL3	PSEL2	PSEL1	PSEL0	Interrupt Source Promoted
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$ (External Pin or Parallel I/O)
0	1	1	1	Real Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5

NOTE:
During reset, PSEL3, PSEL2, PSEL1, and PSEL0 are initialized to 0:1:0:1 which corresponds to "Reserved (default to $\overline{IRQ}$)" being the highest priority I-bit-related interrupt source.

9.3 Low-Power Modes

The MCU contains two programmable low power consumption modes; WAIT and STOP. These two instructions are discussed below. **Table 9-7** summarizes the activity on all pins of the MCU for all operating conditions.

9.3.1 WAIT Instruction

The WAI instruction puts the MCU in a low power consumption mode, keeping the oscillator running. Upon execution of a WAI instruction, the machine state is stacked and program execution stops. The wait state can be exited only by an unmasked interrupt or $\overline{RESET}$. If the I bit is set (interrupts masked) and the COP is disabled, the timer system will be turned off to additionally reduce power consumption. The amount of power savings is application dependent and depends upon circuitry connected to the MCU pins as well as which subsystems (i.e., timer, SPI, SCI) are active when the WAIT mode is entered. Turning off the A/D subsystem by clearing ADPU further reduces WAIT mode current.

9.3.2 STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode provided the S bit in the condition code register is clear. If the S bit is set, the STOP mode is disabled and STOP instructions are treated as NOPs (no operation). In the STOP mode, all clocks including the internal oscillator are stopped causing all internal processing to be halted. Recovery from the STOP mode may be accomplished by $\overline{RESET}$, $\overline{XIRQ}$, or an unmasked $\overline{IRQ}$. When the $\overline{XIRQ}$ is used, the MCU exits from the STOP mode regardless of the state of the X bit in the condition code register; however,

the actual recovery sequence differs depending on the state of the X bit. If the X bit is clear, the MCU starts up with the stacking sequence leading to normal service of the $\overline{XIRQ}$ request. If the X bit is set, then processing will continue with the instruction immediately following the STOP instruction and no $\overline{XIRQ}$ interrupt service routine is requested. A reset will always result in an exit from the STOP mode, and the start of MCU operation is determined by the reset vector.

Table 9-7 Pin State Summary for RESET, STOP, and WAIT

Pins	Single Chip Modes			Expanded Modes		
	RESET	WAIT	STOP	RESET	WAIT	STOP
Output Only						
E	Active E	Active E	0	Active E	Active E	0
XTAL!!!	Active	Active	1	Active	Active	1
STRB/RW	0	SS	SS	1	1	1
PA3-PA6	0	SS	SS	0	SS	SS
PB0-PB7	0	SS	SS	HI ADD	HI ADD	HI ADD
Input/Output						
RESET	I (0)	I	I	I (0)	I	I
MODA/LIR	I (0)	OD (1)	OD (1)	I (1)	OD (1)	OD (1)
MODB/V_{STBY}	I (MODB)	I (V_{STBY})	I (V_{STBY})	I (MODES)	I (V_{STBY})	I (V_{STBY})
STRA/AS	I (STRA)	I (STRA)	I (STRA)	Active AS	Active AS	0
PA7	I	I/O	I/O	I	I/O	I/O
PC0-PC7	I	I/O	I/O	ADD/DATA	SP-8/DATA	LO ADD
PD0-PD5	I	I/O	I/O	I	I/O	I/O
Input Only						
EXTAL	Input Clock or Connect to Crystal with XTAL					
$\overline{IRQ}$	Terminate Unused Inputs to V_{DD}					
$\overline{XIRQ}$	Terminate Unused Inputs to V_{DD}					
PA0-PA2	Terminate Unused Inputs to V_{DD} or V_{SS}					
PE0-PE7	If Not Used, External Drive Not Required					
V_{RH}-V_{RL}	If Not Used, External Drive Not Required					

SYMBOLS:
DATA =Current data present.
I =Input pin, if ( ) associated then this is required input state.
I/O =Input/output pin, state determined by data direction register.
HI ADD =High byte of the address.
LO ADD =Low byte of the address.
ADD/DATA =Low byte of the address multiplexed with data.
OD =Open drain output, ( ) current output state.
SS =Steady state, output pin stays in current state.
SP-8 =Address output during WAI period following WAI instruction, stack pointer value, at time of WAI, minus 8.
!!! =XTAL is output but not normally usable for any output function beyond crystal drive.

Since the oscillator is stopped in the STOP mode, a restart delay of 4064 clock cycle times may be required to allow oscillator stabilization. If the internal oscillator is being used, this delay is required; however, if a stable external oscillator is being used, a control bit in the OPTION register may be used (DLY = 0) to give a delay of four cycles.

APPENDICE C: DIMA DI FORATURA PER MONTAGGIO IN PIGGY-BACK

La scheda può essere interfacciata in due modi, un modo é quello del montaggio in piggy-back, in quanto la scheda monta dei connettori CN1 e CN5, che sul lato saldature hanno i pin sporgenti di 7 mm, quindi é possibile realizzare una connessione con delle strip femmina.
Il secondo modo consiste nell'inserire la scheda, da sola o con altre schede (tipo ZBRxxx o ZBT xxx), su una guida Weidmuller tipo RS/100 codice 414487, per montaggio a Ω tipo DIN 46277-1 e DIN 46277-2.

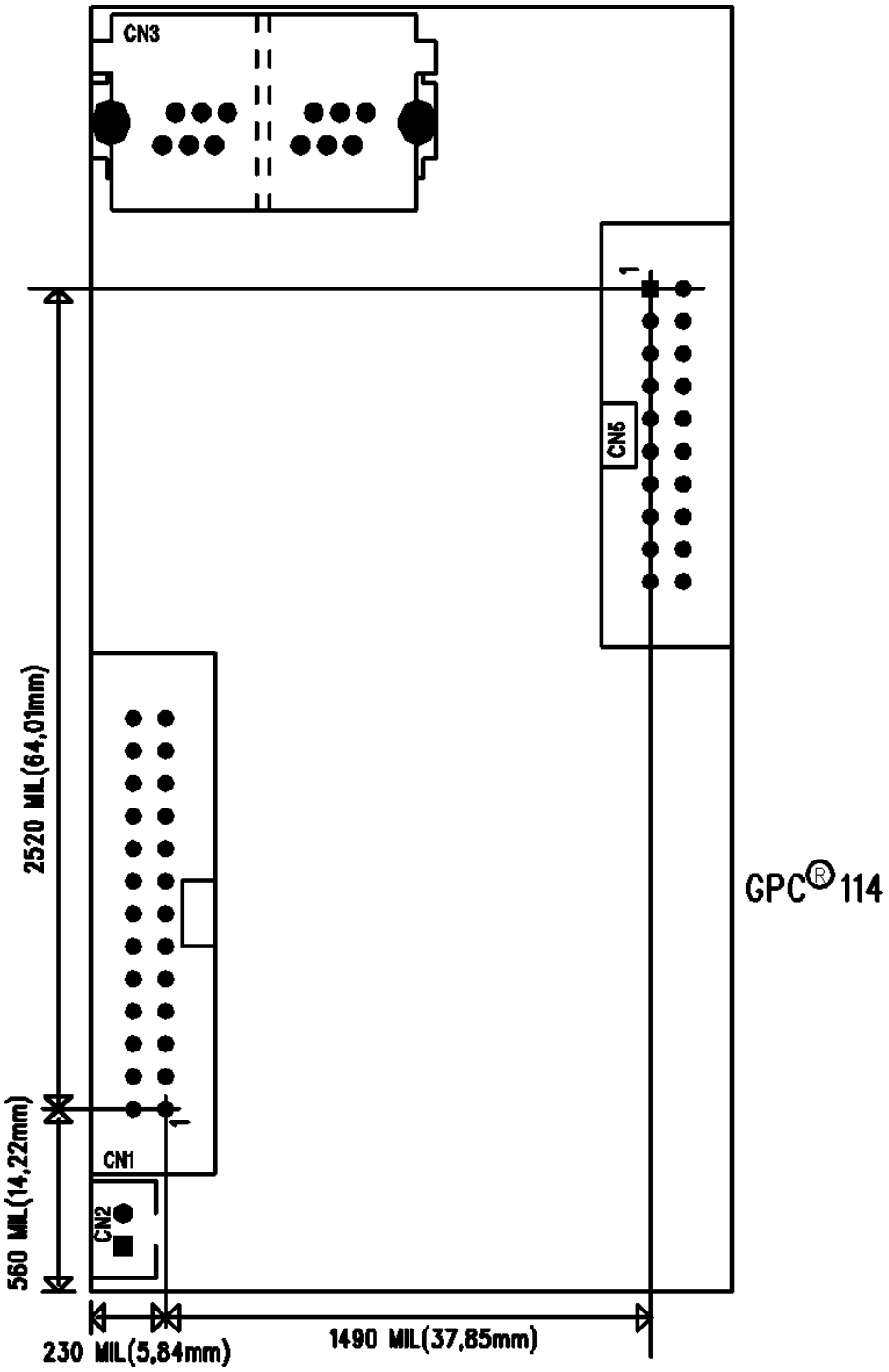


FIGURA 31: DIMA DI FORATURA PER MONTAGGIO IN PIGGY-BACK

APPENDICE D: SCHEMI ELETTRICI

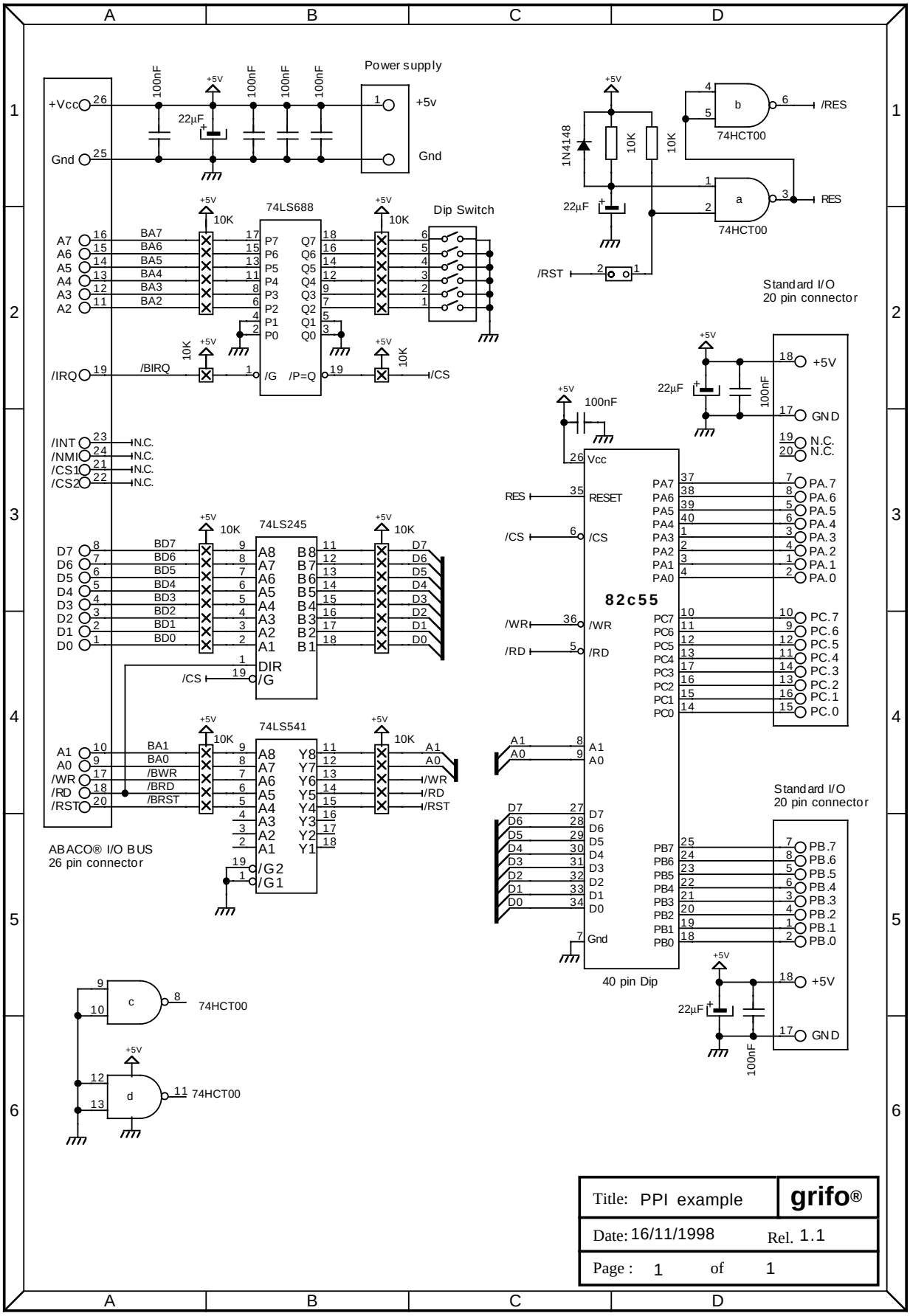


FIGURA 32: SCHEMA ELETTRICO DI ESPANSIONE PPI

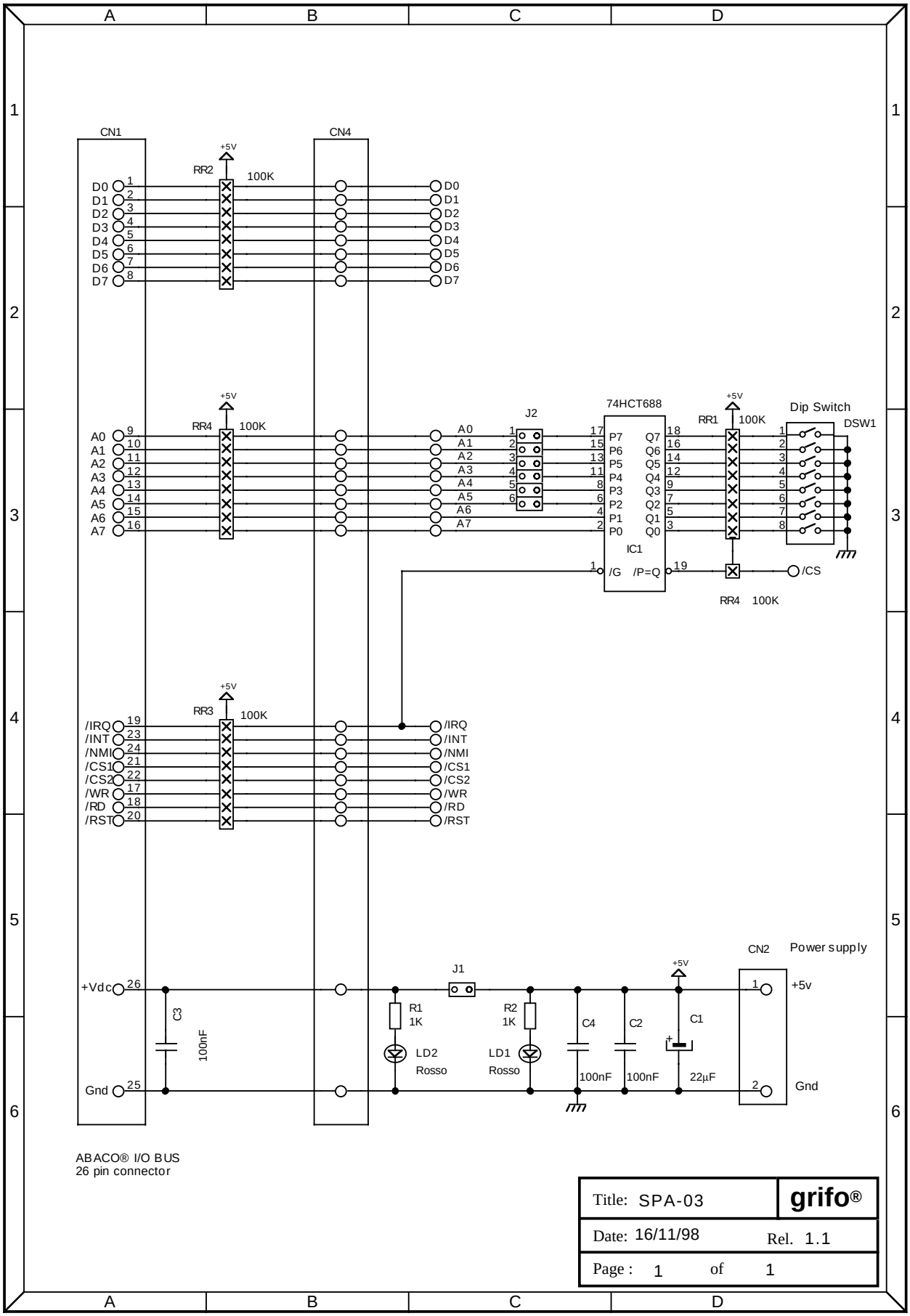


FIGURA 33: SCHEMA ELETTRICO SPA-03

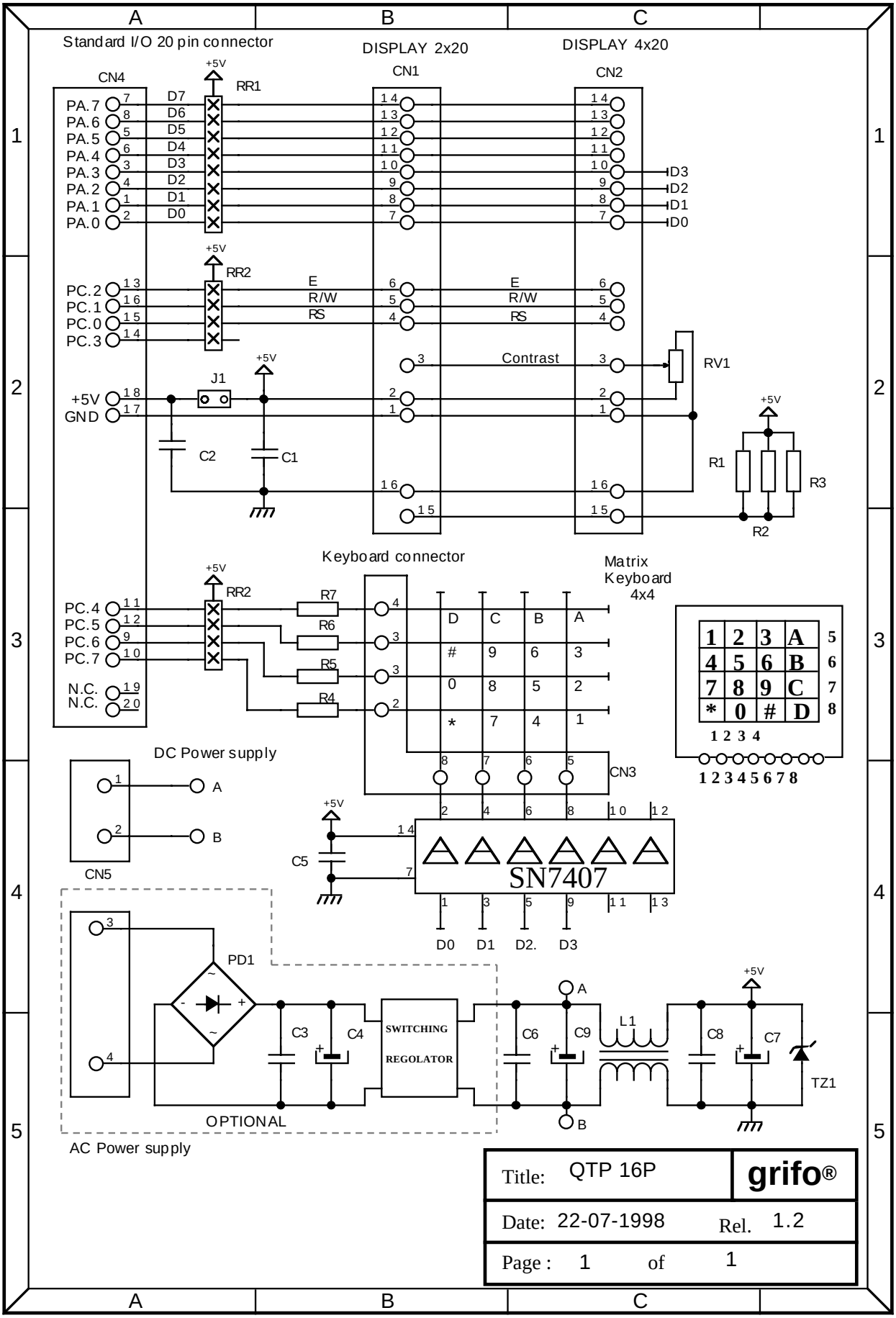


FIGURA 34: SCHEMA ELETTRICO QTP-16P

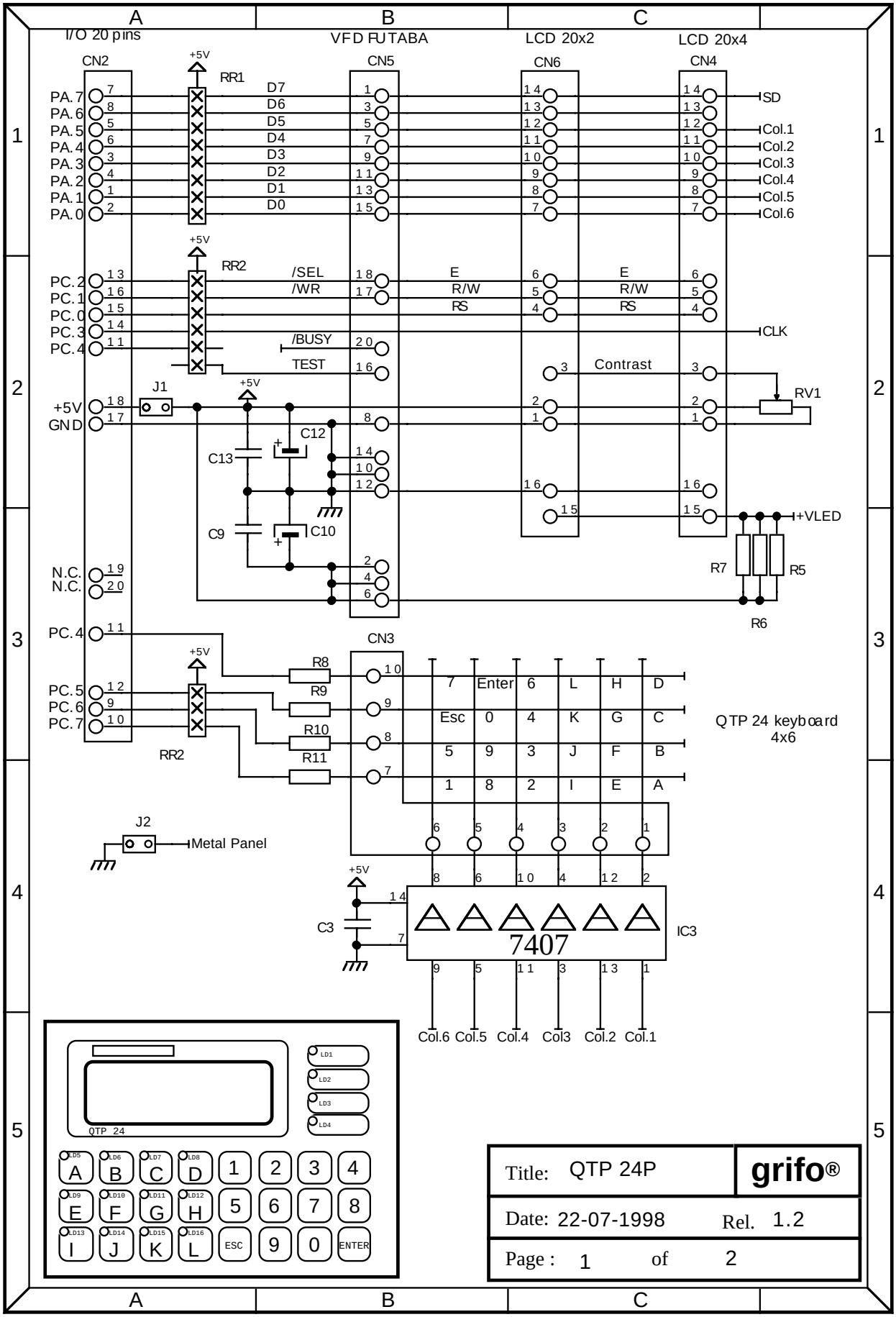


FIGURA 35: SCHEMA ELETTRICO QTP-24P 1/2

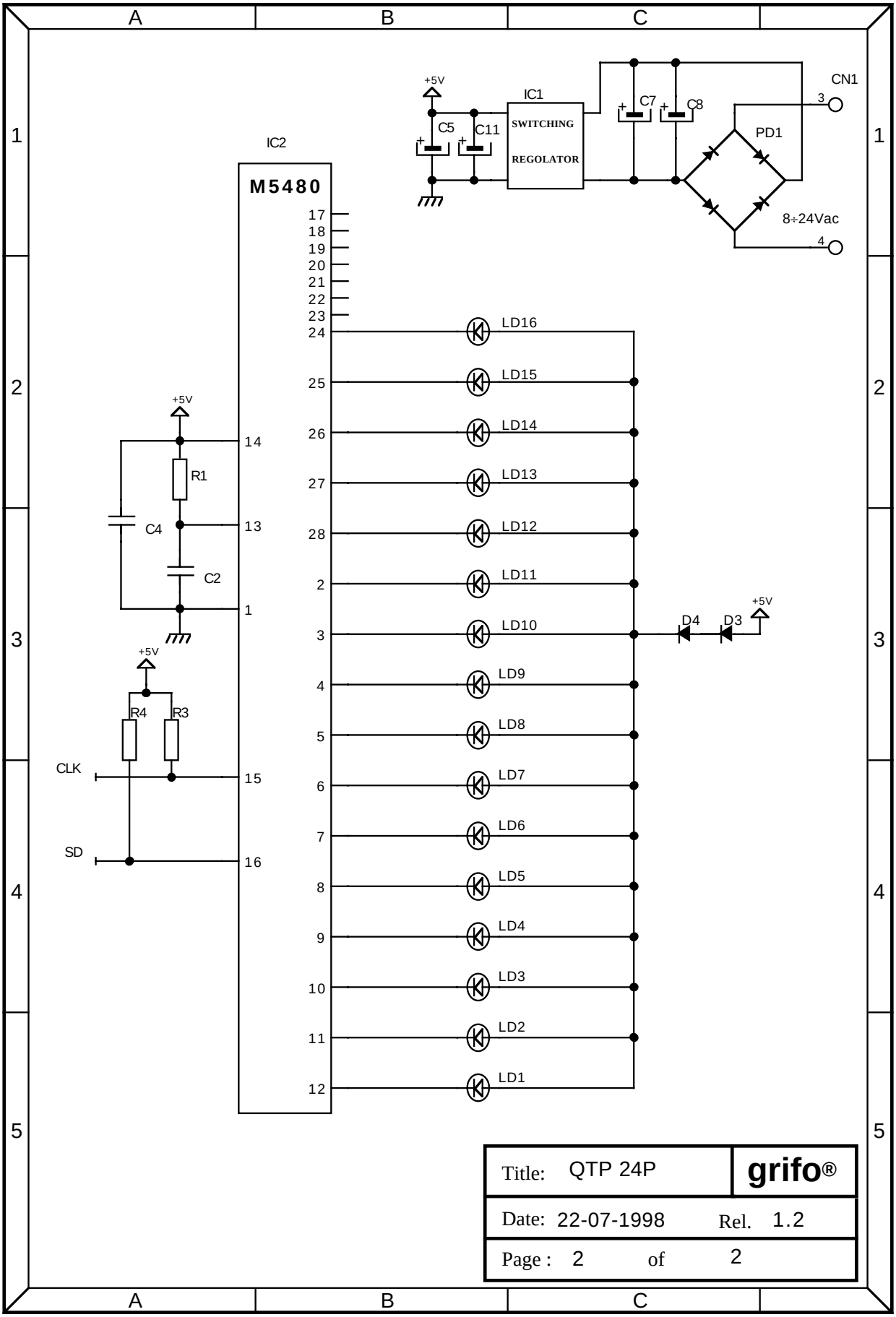


FIGURA 36: SCHEMA ELETTRICO QTP-24P 2/2

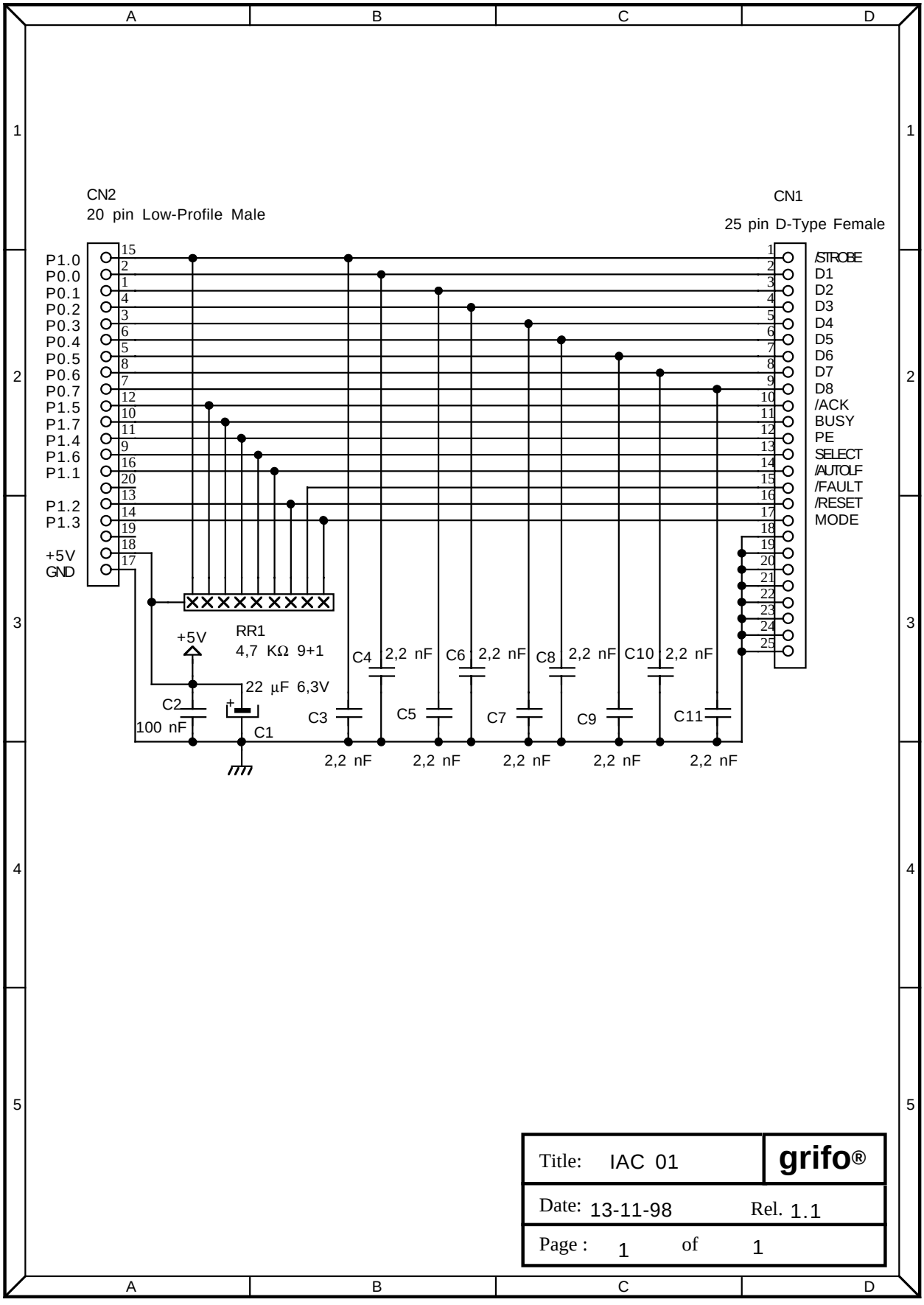


FIGURA 37: SCHEMA ELETTRICO IAC-01

APPENDICE E: INDICE ANALITICO

V

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